

PREFACE

The IBM Personal Computer Technical Reference Manual is designed to provide hardware design and interface information. This publication also provides Basic Input Output System (BIOS) information as well as programming support matter.

This manual is intended for programmers, engineers involved in hardware and software design, designers, and interested persons who have a need to know how the IBM Personal Computer is designed and works.

This manual has three sections:

Section-1

"HARDWARE OVERVIEW," features an overview of the system as a whole calling out specific items such as the System Unit, Keyboard, IBM Monochrome Display and the 80 CPS Graphics Printer.

Section-2

"HARDWARE," contains a description for each functional part of the system. This section also contains specifications for power, timing, and interface. Programming considerations are supported by coding tables, command codes and registers.

Section-3

"ROM and SYSTEM USAGE," describes BIOS as well as how to use BIOS, interrupt vector listings, memory map, vectors with special meanings, a cassette section, a keyboard encoding section, and a set of Low Memory Maps.

"APPENDICES," to address the ROM BIOS listing, an instruction set, logic diagrams, and expanded charts used to support specific hardware descriptions.



Technical Reference

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The IBM Personal Computer has two major elements; a System Unit and a keyboard. In addition, a variety of options are offered including one or two 5-1/4" Diskette Drives with adapter which can be housed inside the System Unit, an IBM Monochrome Display, an IBM 80 CPS Graphics Printer, two display adapters, storage increments to 544KB, an Asynchronous Communications Adapter, Printer Adapter and a Game Control Adapter.

The System Unit is the heart of your IBM Personal Computer system. The System Unit houses the microprocessor, Read-Only Memory (ROM), Read/Write Memory, Power Supply, and System Expansion Slots for the attachment of up to five options. One or two 5-1/4" Diskette Drives can also be mounted in the System Unit providing 160KB or 320 KB of storage each, depending on the type of drive you have.

The System Board is a large board which fits horizontally in the base of the System Unit and includes the microprocessor, 40KB ROM and 16KB memory. The memory can be expanded in 16KB increments to 64KB. The System Board also includes an enhanced version of the Microsoft BASIC-80 Interpreter without diskette functions. The BASIC Interpreter is included in the ROM. The System Board also permits the attachment of an audio cassette recorder for loading or saving programs and data.

The System Unit power supply is a 63.5 watt, 4 level DC and either 120 Vac or 220/240 Vac unit. It is a switching regulator design, allowing for light weight and high efficiency. Its DC power capacity is rated for an expanded system.

The 5-1/4" Diskette Drive permits the IBM Personal Computer to read, write and store data on 5-1/4" diskettes. Each diskette stores approximately 160KB or 320KB of formatted data. Two of these drives may be installed internally in the System Unit.

The keyboard is attached to the System Unit with a light-weight, coiled cable. The keyboard features 83 keys, and offers commonly used data and word processing functions in a design combining the familiar typewriter and calculator pad layouts.

A base system requires one of two different display adapters, either a Color/Graphics medium resolution Monitor adapter or a high resolution monochrome alphanumeric adapter with a parallel printer adapter.

The Color/Graphics Adapter operates at U.S. NTSC (National Television System Committee) standard frequencies (15,750 Hz horizontal and 60 Hz vertical scan), allowing direct attachment to a variety of home TVs (with a user supplied RF modulator) and monitors.

The Color/Graphic Monitor adapter supports a variety of modes selected by program control. The adapter supports color or black and white alphanumeric modes with line width of 40 or 80 characters and 25 lines. In the alphanumeric mode there are 256 characters.

This adapter provides both a standard composite video and direct drive outputs. In addition, a light pen feature input port is provided.

The IBM Monochrome Display is a high resolution green phosphor display offering the personal computer user quality usually found on larger computer systems. The display features an 11-1/2" screen with an anti-glare surface and a variety of highlighting choices. The screen displays 25 lines of 80 characters. It supports 256 different letters, numbers and special characters that are formed in a nine by 14 dot matrix.

The IBM Monochrome Display requires the Monochrome Display and Printer Adapter Option. This option installs in one of the System Unit's five System Expansion Slots. The display is powered from the System Unit.

The IBM 80 CPS Graphics Printer is a versatile, low cost, quality printer. It prints in both directions at a nominal horizontal speed of 80 characters per second on continuous-feed, single or multipart paper. The printer features four character sizes (40, 66, 80, or 132 characters per line), subscript, superscript, and underlining. It has uppercase and lowercase ASCII and International character sets, a defined graphic character set and programmable graphics. In addition it has a Power-on Self-test, simple paper loading and a cartridge ribbon.

The IBM 80 CPS Graphics Printer requires either the Monochrome Display and Printer Adapter or the Printer Adapter installed in one of the System Unit's five System Expansion Slots. The printer is available in either a 120 volt, 60 Hz version or a 220 or 240 volt, 50/60 Hz version and plugs into a standard wall outlet. The printer requires the Printer Cable Option for attachment to the System Unit.

The 16KB Memory Module Kits allow you to increase the memory size of your IBM Personal Computer. The base system comes standard with 16KB of memory. Up to three 16KB Memory Module Kits may be installed to increase the memory size to 64KB. Memory can be further increased to 544KB with additional memory options once these three Expansion Kits are installed.

The 16KB Memory Kits plug into the System Board and must be installed sequentially. They do not occupy any of the five System Expansion Slots.

The 32KB, 64KB, and 64/256KB Memory Expansion Options permit memory capacity to be increased beyond 64KB. Any combination of up to three Memory Expansion Options may be installed as long as System Expansion Slots are available. A maximum of 480KB of Memory Expansion Options can be addressed, which when added to 64KB on the System Board, gives a total memory capacity of 544KB.

Each 32KB, 64KB, or 64/256KB Memory Expansion Option requires a System Expansion Slot in the System Unit. The first 64KB on the System Board is required before any Memory Expansion Options can be installed.

The 64KB Memory Module Kits allow the memory size of a 64/256KB Memory Expansion Option to be increased. Each 64KB Kit consists of 9 modules which plug into the 64/256KB Option and must be installed sequentially. The base 64/256KB Option comes standard with 64KB of memory. One, two, or three 64KB Kits may be added, providing the 64/256KB Option with 128KB, 192KB, or 256KB of memory respectively.

The Asynchronous Communications Adapter provides a channel to data processing or input/output devices outside of your immediate system. These can be connected by telephone using a plug-in modem, or directly by cable when the device is nearby.

This option utilizes the RS232C asynchronous (start-stop) interface permitting attachment to a variety of devices including a large "host" computer or another IBM Personal Computer.

This option supports 50 to 9600 BPS transmission speeds. One 25 pin "D" shell, male type connector is provided to attach various peripheral devices. A "current loop" interface is located in the same connector, and a jumper block is provided to manually select either the voltage or the current loop interface.

The Asynchronous Communications Adapter requires a System Expansion Slot in the System Unit. Telephone line transmission requires an external modem which is subject to local telephone administration and national regulations. Note that references to local telephone administration and national regulations should not be taken to imply that permission to connect has been, or will be, obtained in any particular country.

The Game Control Adapter permits the attachment of user-supplied Joysticks or paddles. Two Joysticks and up to four paddles may be attached. IBM does not manufacture either the Joysticks or the paddles. This option provides connectors for Joysticks or paddles and requires a System Expansion Slot in the System Unit.

A block diagram of the system is on the following pages (1-6 and 1-7).

The Prototype Card is provided by IBM for those who wish to design a customized option for the IBM Personal Computer. The Prototype Card is inserted into an expansion slot in the System Unit.

System Block Diagram

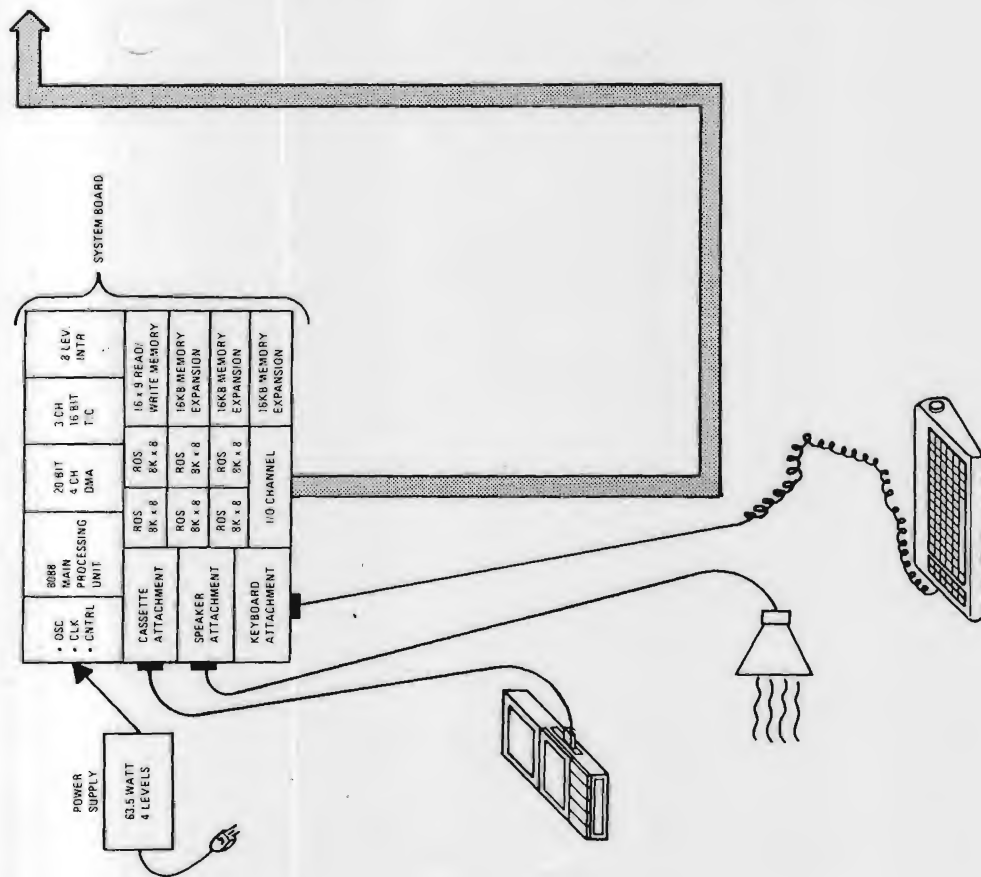


Figure 1. SYSTEM BLOCK DIAGRAM

OVERVIEW

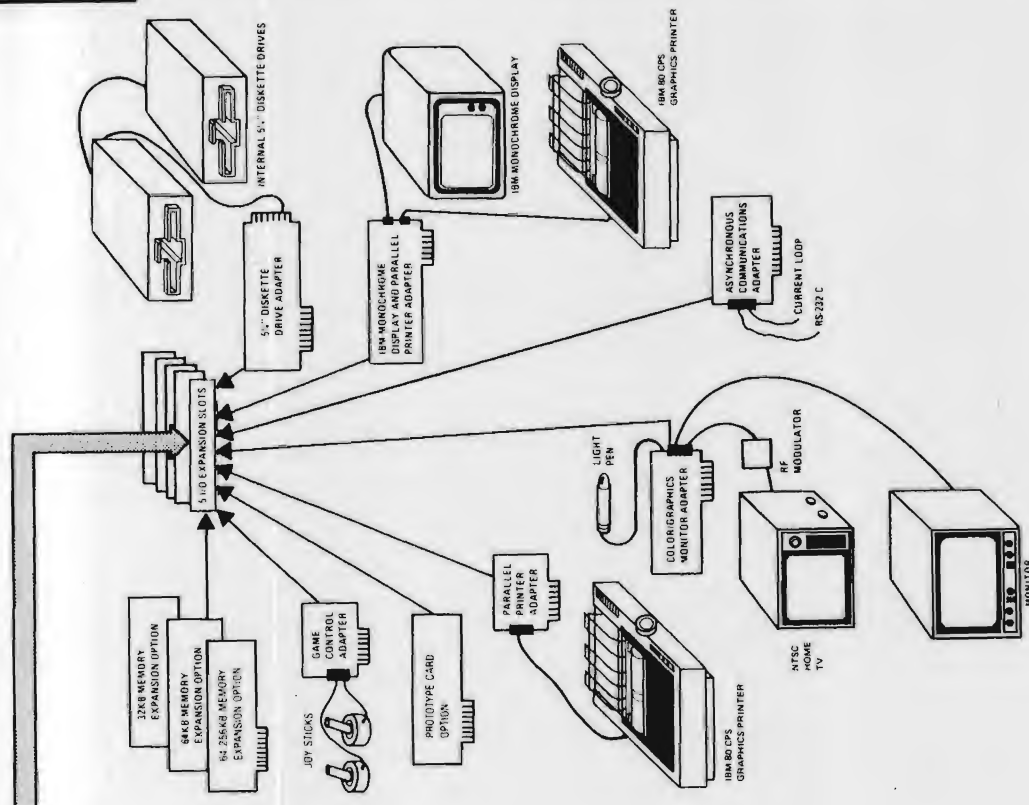


Figure 1. SYSTEM BLOCK DIAGRAM (continued)

System Board

The System Board fits horizontally in the base of the System Unit and has dimensions of approximately 8-1/2 inches by 11 inches. The System Board is a multilayer single land-per-channel design, with ground and power internal planes provided. DC power and a signal from the power supply enter the board through two six pin connectors. Other connectors on the board are for attaching the keyboard, audio cassette, and the speaker. Five 62-pin card edge sockets are also mounted on the System Board. The system I/O channel is bussed across these five I/O slots.

There are 16 (13 used) Dual In-line Package (DIP) switches mounted on the card which can be read under program control. These switches are used to indicate to the system software what options are installed. They are used to indicate amounts of installed storage, both on the System Board and in the System Expansion slots, type of display adapter installed, and desired operation modes upon power-up; ie, color or black and white and 80- or 40 character lines. Switches are also used to identify when the operating system is to be loaded from diskette, and how many diskette drives are attached.

The major elements of the System Board are divided into five major functional areas. They are, the processor subsystem and its support elements, the Read-Only Memory (ROM) subsystem, the Read/Write (R/W) Memory subsystem, integrated I/O adapters, and the I/O channel. All functions are described in detail in this section, except for the I/O channel, which has its own section. Figure 2.0 "System Board Data Flow" page 2-6, illustrates these functional areas.

The heart of the System Board is the Intel 8088 microprocessor. This processor is an 8-bit bus version of the 16-bit 8086 processor by Intel. It is software compatible with the 8086 and, thus, supports 16-bit operations including multiply and divide. The processor supports 20 bits of addressing (1 megabyte of storage). The processor is implemented in maximum mode so a co-processor can be added as a feature. The processor is operated at 4.77 Mhz. This frequency is derived from a 14.31818 Mhz crystal which is divided by three for the processor clock and by four to obtain the 3.58 Mhz color burst signal required for color televisions. At the 4.77 Mhz clock rate, the 8088 bus cycles are four clocks of 210 ns or 840 ns. I/O cycles take five 210 ns clocks or 1.05 microsec (m sec).

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HARDWARE

HARDWARE

The processor is supported by a set of high function support devices providing four channels of 20-bit Direct Memory Access (DMA), three 16-bit timer counter channels, and eight prioritized interrupt levels.

Three of the four DMA channels are available on the I/O bus and are provided to support high speed data transfers between I/O devices and memory without processor intervention. The fourth DMA channel is programmed to refresh the system dynamic memory. This is done by programming a channel of the timer counter device to periodically request a dummy DMA transfer. This creates a memory read cycle which is available to refresh dynamic storage both on the System Board and in the System Expansion slots. All DMA data transfers, except the refresh channel, take five processor clocks of 210 ns or 1.05 ns if the processor ready line is not deactivated. Refresh DMA cycles take four clocks or 840 ns.

The three timer/counters are used by the system as follows: Channel 0 is used to time and request refresh cycles from the DMA channel, Channel 2 is used to support the tone generation for the audio speaker, and Channel 1 is used by the system as a general purpose timer providing a constant time base for implementing a time-of-day clock. Each channel has a minimum timing resolution of 1.05 μ sec.

Of the eight prioritized levels of interrupt, six are bussed to the I/O slots for use by feature cards. Two levels are used on the System Board. Level 0, the highest priority, is attached to Channel 1 of the timer counter and provides a periodic interrupt. Level 1 is attached to the keyboard adapter circuits and receives an interrupt for each scan code sent by the keyboard. The Non-Maskable Interrupt (NMI) of the 8088 is used to report memory parity errors.

The System Board is designed to support both ROM and Read/Write Memory. The System Board contains space for 48K x 8 of ROM or EPROM. Six module sockets are provided, each capable of accepting an 8K x 8 device. Five of the sockets are populated with 40KB of ROM. This ROM contains the Cassette BASIC interpreter, cassette operating system, Power-on Self-test, I/O drivers, dot patterns for 128 characters in graphics mode, and a diskette bootstrap loader. The ROM is packaged in 24-pin modules and has an access time of 250ns and a cycle time of 375 ns.

The System Board also contains from 16K x 9 to 64K x 9 of Read/Write Memory. A minimum system would have 16KB of memory with module sockets for an additional 48KB. In a cassette version of the system, approximately 4KB is used by the system leaving approximately 12KB of user's space for BASIC programs. Additional memory beyond the System Board's maximum of 64KB, is obtained by adding memory cards in the System Expansion slots.

The memory is dynamic 16K x 1 chips with an access time of 250 ns and a cycle time of 410 ns. All R/W memory is parity checked. The System Board contains circuits for attaching an audio cassette, the serial keyboard, and the speaker. The cassette adapter allows the attachment of any good quality audio cassette via either the microphone or auxiliary inputs. The board has a jumper for either input. This interface also provides a cassette motor control line for transport starting and stopping under program control. This interface reads and writes the audio cassette at a data rate of between 1,000 and 2,000 baud. The baud rate is variable and dependent on data content since a different bit-cell time is used for 0's and 1's. For diagnostic purposes, the tape interface can loop read to write to test the board's circuits. The system software blocks cassette data, generates and checks data with a Cyclic Redundancy Check (CRC).

The processor also contains the adapter circuits for attaching the serial interface from the keyboard. This generates an interrupt to the processor when a complete scan code is received. This interface can request execution of a diagnostic in the keyboard.

Both the keyboard and cassette interfaces are provided via 5-pin DIN connectors, which are right angle mounts on the System Board and extend through the rear panel of the System Unit.

The system is provided with a 2-1/4 inch audio speaker mounted inside the System Unit. The System Board contains the control circuits and driver for the speaker. The speaker connects through a 2-wire interface which attaches to a 4-pin header on the System Board.

The speaker drive circuit is capable of approximately a 1/2 watt of power. The control circuits allow the speaker to be driven several different ways. First, a direct program control register bit may be toggled to generate a pulse train; second, the output of Channel 2 of the timer counter may be programmed to generate a waveform to the speaker. Third, the clock input to the timer/counter can be modulated with a program controlled I/O Register Bit. All three forms of control may be performed simultaneously.

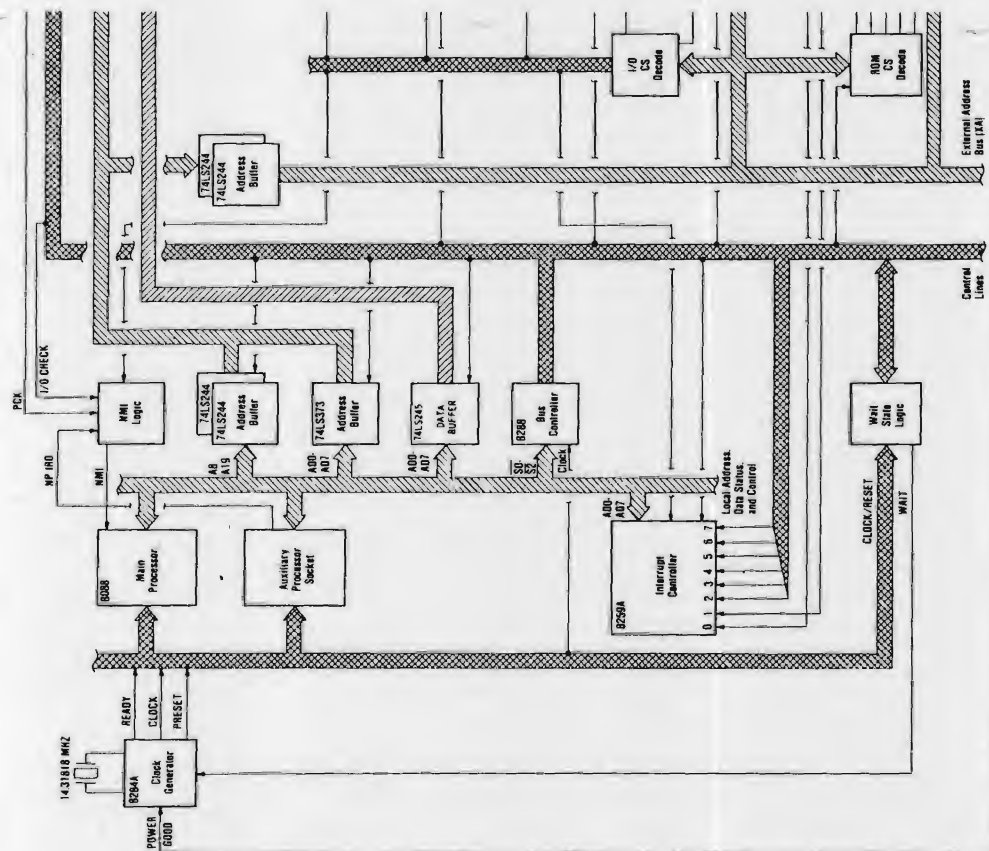


Figure 2. SYSTEM BOARD DATA FLOW (SHEET 1 OF 2)

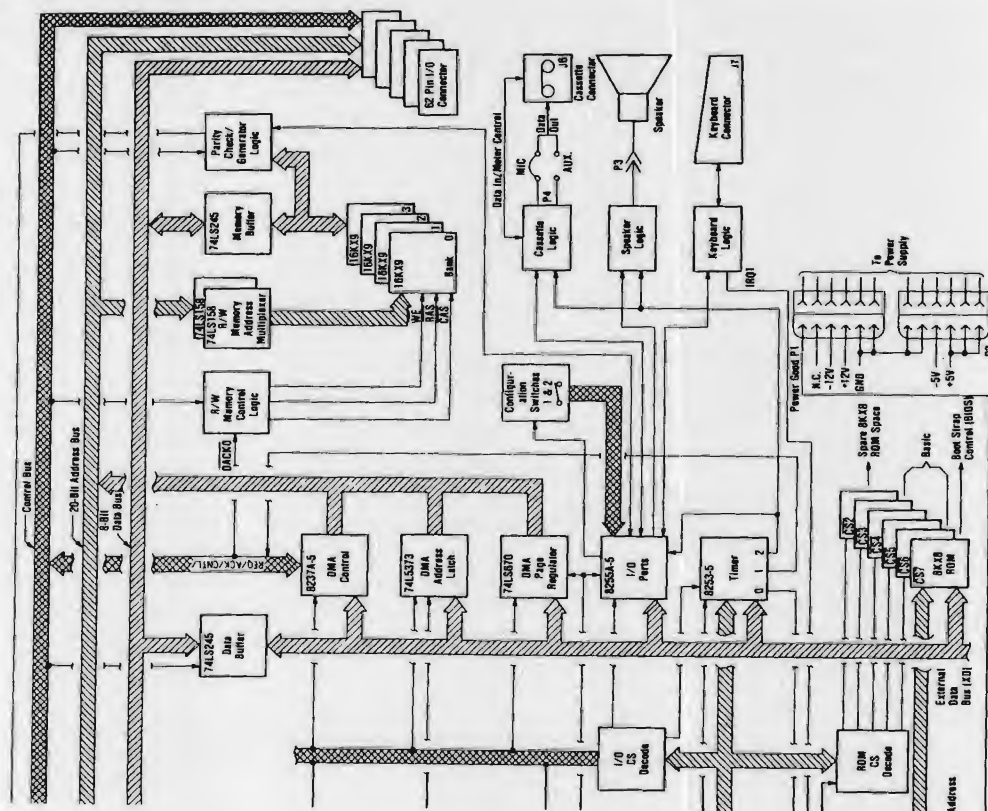


Figure 2. SYSTEM BOARD DATA FLOW (SHEET 2)

I/O Channel

The I/O channel is an extension of the 8088 microprocessor bus. It is, however, demultiplexed, repowered, and enhanced by the addition of interrupts and Direct Memory Access (DMA) functions. The I/O channel contains an 8-bit bidirectional data bus, 20 address lines, 6 levels of interrupt, control lines for memory and I/O read or write, clock and timing lines, 3 channels of DMA control lines, memory refresh timing control lines a channel check line, and power and ground for the adapters. Four voltage levels are provided for I/O card +5 Vdc, -5 Vdc, +12 Vdc, and -12 Vdc. These functions are provided in a 62-pin connector with 100 mil card tab spacing.

A ready line is available on the I/O channel to allow operation with slow I/O or memory devices. If the channel's Ready line is not activated by an addressed device, all processor generated memory read and write cycles take four 210 ns clock or 840 ns/byte. All processor-generated I/O read and write cycles require five 210 ns clocks or 1.05 m sec/byte. All DMA transfers require five clocks for a cycle time of 1.05 m sec/byte. Refresh cycles are present once every 72 clocks or approximately 15 m sec and require five clocks or approximately 7% of the bus bandwidth. I/O devices are addressed using I/O mapped address space. The channel is designed so that 512 I/O device addresses are available to the I/O channel cards.

A channel check line exists for reporting error conditions to the processor. Activating this line results in a NMI to the 8088 processor. Memory Expansion Options use this line to report parity errors.

The I/O channel is repowered so there is sufficient drive to power all five System Expansion Slots, assuming two loads per slot. The IBM Option I/O adapters typically use only one load. A graphic illustration of the System I/O Channel and its descriptions are on the following pages.

I/O Channel Diagram

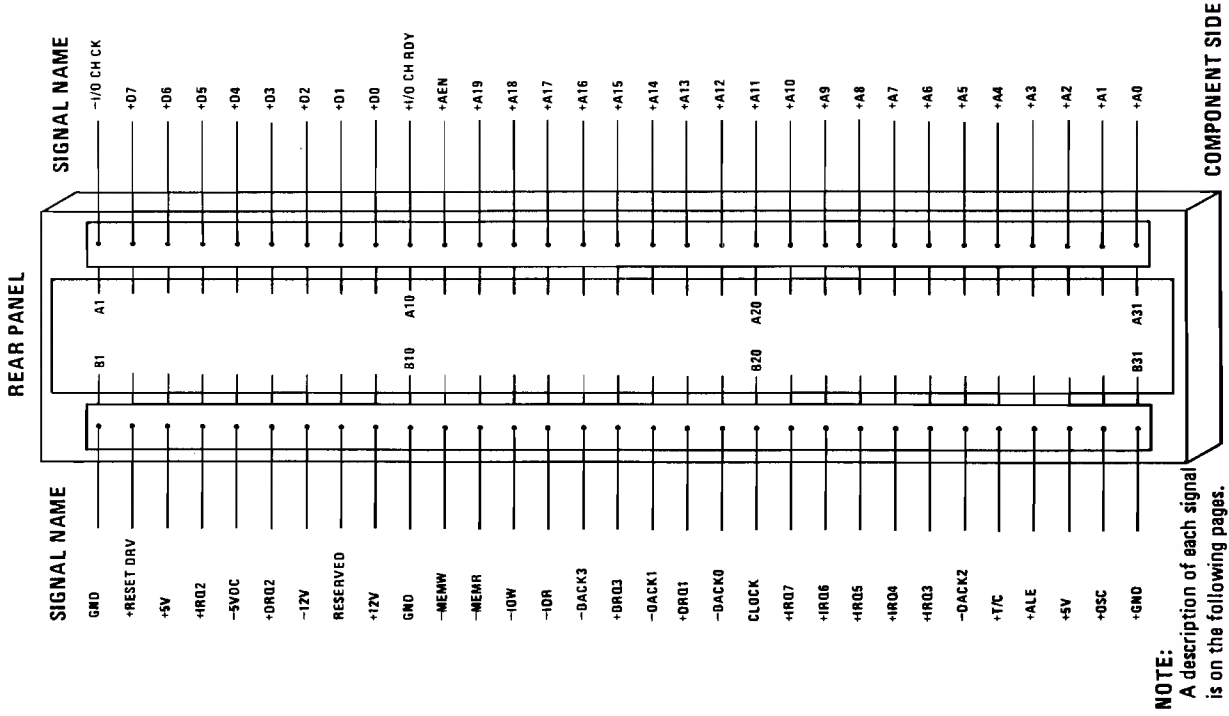


Figure 3. I/O CHANNEL DIAGRAM

System Board I/O Channel Description

The following is a description of the IBM Personal Computer System Board I/O Channel. All signal lines are TTL compatible.

Signal	I/O	Description
OSC	O	Oscillator: This signal is a high speed clock with a 70 nsec. period (14.31818 MHz). It has a 50% duty cycle.
CLK	O	Clock: This is the system clock. It is a divide - by - three of the oscillator and has a period of 210 nsec. (4.77 Mhz.) The clock has a 33% duty cycle.
RESET DRV	O	Reset Driver: This line is used to reset or initialize system logic upon power-up or during a low line voltage outage. This signal is synchronized to the falling edge of clock and is active HIGH.
A0-A19	O	Address Bits 0 to 19: These lines are used to address memory and I/O devices within the system. The 20 address lines allow access of up to 1 megabyte of memory. A0 is the Least Significant Bit (LSB) while A19 is the Most Significant Bit (MSB). These lines are generated by either the processor or the DMA Controller. They are active HIGH.
D0-D7	I/O	Data Bits 0 to 7: These lines provide data bus bits 0 to 7 for the processor, memory, and I/O Devices. D0 is the Least Significant Bit (LSB) and D7 is the Most Significant Bit (MSB). These lines are active HIGH.
ALE	O	Address Latch Enable: This is provided by the 8288 Bus Controller and is used on the System Board to latch valid addresses from the processor. It is available to the I/O Channel as an indicator of a valid processor address (when used in conjunction with AEN). Processor addresses are latched with the falling edge of ALE.
<u>I/O CH CK</u>	I	-I/O Channel Check: This line provides the CPU with parity (error) information on memory or devices in the I/O Channel. When this signal is active LOW, a parity error is indicated.

Signal	I/O	Description
<u>I/O CH RDY</u>	I	I/O Channel Ready: This line (normally high or "READY") is pulled low ("NOT READY") by a memory or I/O device to lengthen I/O or memory cycles. It allows slower devices to attach to the I/O Channel with a minimum of difficulty. Any slow device using this line should drive it low immediately upon detecting a valid address and a Read or Write command. This line should never be held low for any period in excess of 10 clock cycles (2.1 usec.) Machine cycles (I/O or memory) are extended by an integral number of CLK cycles (210 ns).
<u>IRQ2-IRQ7</u>	I	Interrupt Request 2 to 7: These lines are used to signal the processor that an I/O device requires attention. They are prioritized with IRQ2 as the highest priority and IRQ7 as the lowest. An Interrupt Request is generated by raising an IRQ line (Low to High) and holding it high until it is acknowledged by the processor (Interrupt Service Routine).
<u>IOR</u>	O	-I/O Read Command: This command line instructs an I/O device to drive its data onto the data bus. It may be driven by the processor or the DMA Controller. This signal is active LOW.
<u>IOW</u>	O	-I/O Write Command: This command line instructs an I/O device to read the data on the data bus. It may be driven by the processor or the DMA Controller. This signal is active LOW.
<u>MEMR</u>		-Memory Read Command: This command line instructs the memory to drive its data onto the data bus. It may be driven by the processor or the DMA Controller. This signal is active LOW.
<u>MEMW</u>	O	-Memory Write Command: This command line instructs the memory to store the data present on the data bus. It may be driven by the processor or the DMA Controller. This signal is active LOW.

Signal I/O Description

- DRQ1-DRQ3** I DMA Request 1 to 3: These lines are asynchronous channel requests used by peripheral devices to gain DMA service. They are prioritized with DRQ1 having highest priority and DRQ3 the lowest. A request is generated by bringing a DRQ line to an active level (HIGH). A DRQ line must be held high until the corresponding DACK line goes active.
- DACK0-DACK3** O -DMA Acknowledge 0 to 3: These lines are used to acknowledge DMA requests (DRQ1-DRQ3) and to refresh system dynamic memory (DACK0). They are active LOW.
- AEN** O Address Enable: This line is used to degate the processor and other devices from the I/O Channel to allow Direct Memory Access (DMA) transfers to take place. When this line is active (HIGH), the DMA Controller has control of the address bus, data bus, read command lines, (memory and I/O), and the write command lines, (memory and I/O).
- T/C** O Terminal Count: This line provides a pulse when the terminal count for any DMA channel is reached. This signal is active HIGH.

The following voltages are available on the System Board I/O Channel:

- +5 Vdc \pm 5%, Located on 2 connector pins.
- 5 Vdc \pm 10%, Located on 1 connector pin.
- +12 Vdc \pm 5%, Located on 1 connector pin.
- 12 Vdc \pm 10%, Located on 1 connector pin.
- GND (Ground), Located on 3 connector pins.

System Board Component Diagram

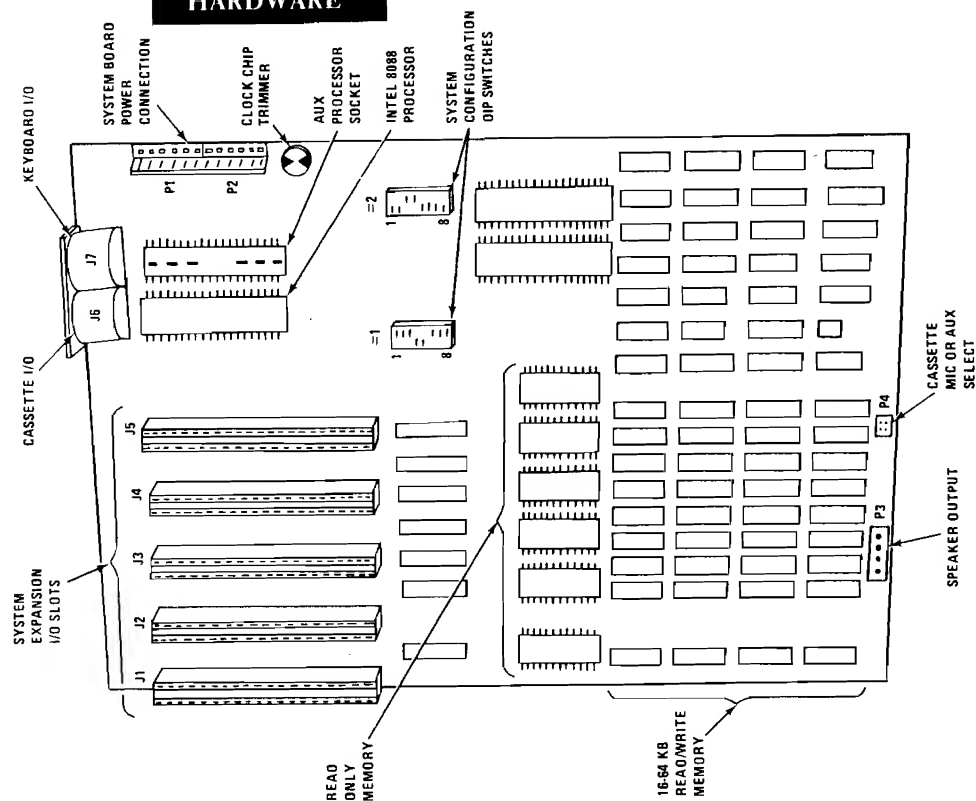


Figure 4. SYSTEM BOARD COMPONENT DIAGRAM

Keyboard

The Keyboard is a device separate from the System Unit. It is attached via a serial interface cable approximately 6 feet in length which plugs into the rear of the System Unit. The attaching cable is coiled, like that of a telephone headset, and is a shielded four-wire wire connection. The interface contains power (+5 Vdc), ground and two bidirectional signal lines. The cable is permanently attached at the keyboard end and plugs into the System Unit via a DIN connector.

The keyboard uses a capacitive technology with a microcomputer (Intel 8048) performing the keyboard scan function. The keyboard interface is defined so system software has the maximum flexibility in defining keyboard operations such as shift states of keys, make/break keys, and typematic operation. This is accomplished by having the keyboard return scan codes rather than American Standard Code for Information Interchange (ASCII) codes. In addition, all keys except control keys are typematic and generate both a make and a break scan code. For example, key 1 produces scan code 01 on make, and code 81 on break. Break codes are formed by adding X'80' to make codes. The keyboard I/O driver can define keyboard keys as shift or typematic keys as required by the application.

The microcomputer (Intel 8048) in the keyboard performs several functions including a Power-on Self-test and when requested by the System Unit. This diagnostic CRC checks the microcomputer ROM, tests memory and checks for stuck keys. Additional functions are: keyboard scanning, key debounce, buffering of up to 20 key scan codes, maintaining bidirectional serial communications with the System Unit, and executing the hand shake protocol required by each scan code transfer. A keyboard diagram and table of scan codes are on the following pages. Figure (5) is a block diagram of the keyboard interface on the System Board.

Several different keyboard arrangements are available. These are illustrated on the following pages together with a table of scan codes for the U.S. keyboard. For information on the keyboard routines required to implement non-U.S. keyboards, refer to the Guide to Operations and DOS manuals.

Note: Reference to local telephone administration and national regulations should not be taken to imply that permission to connect has been, or will be, obtained in any particular country.

Keyboard Interface Block Diagram

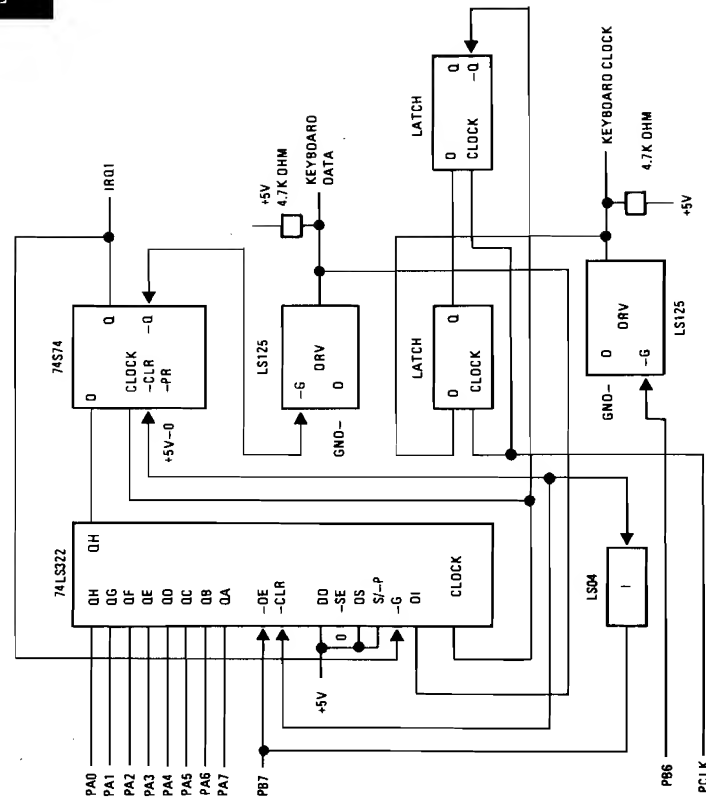
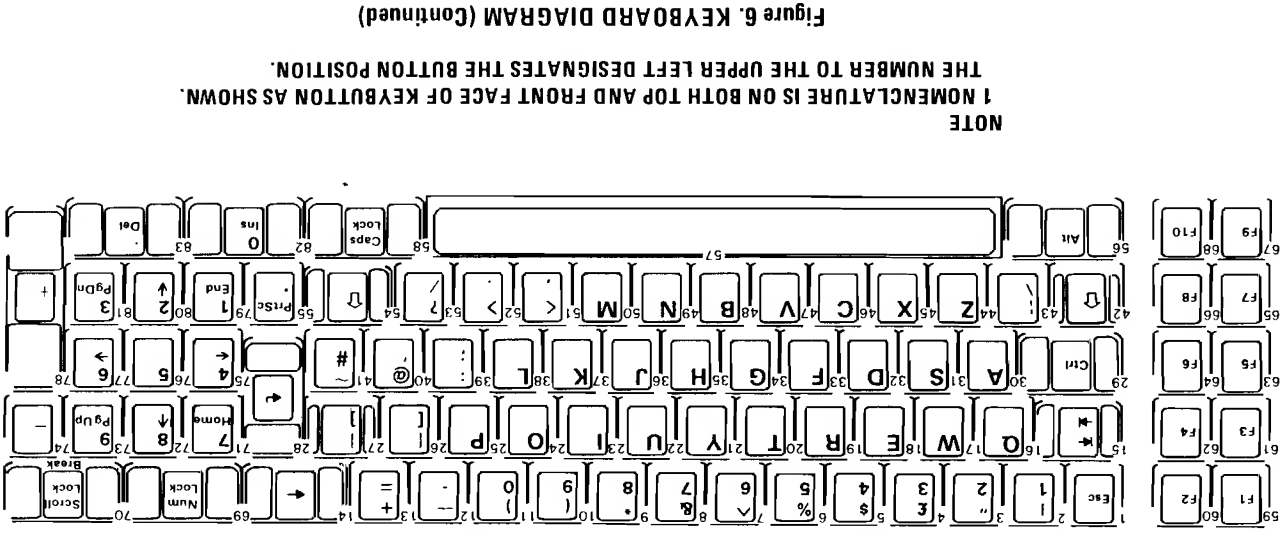


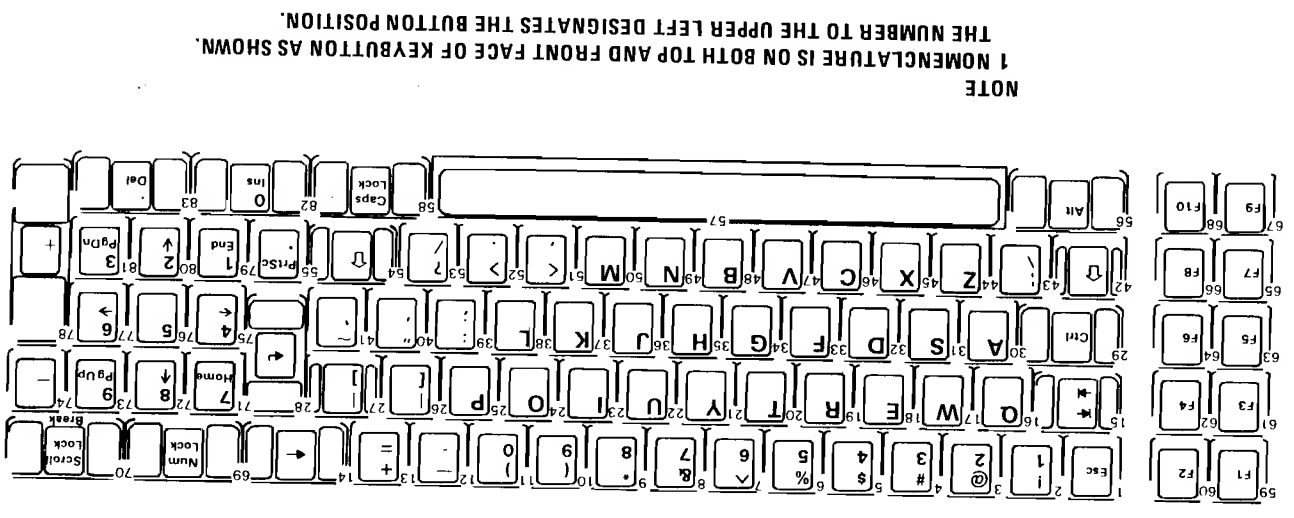
Figure 5. KEYBOARD INTERFACE BLOCK DIAGRAM

United Kingdom Keyboard Diagram



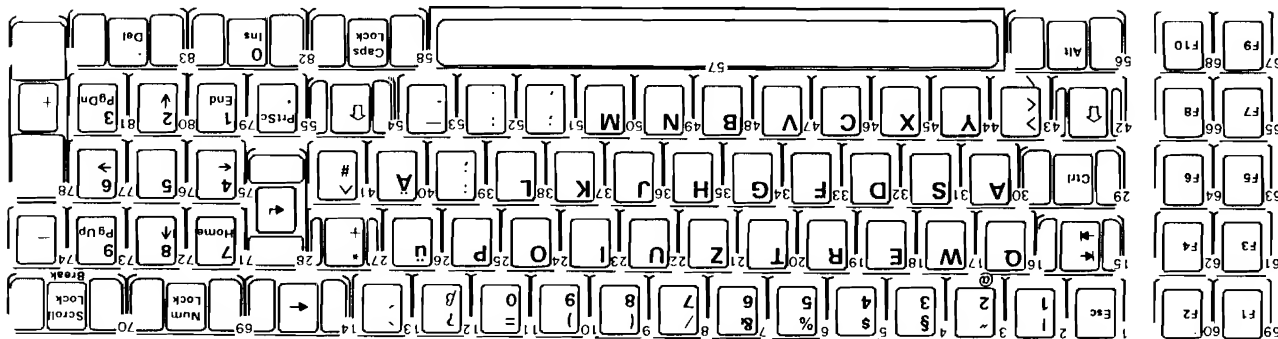
NOTE
1 NOMENCLATURE IS ON BOTH TOP AND FRONT FACE OF KEYBUTTON AS SHOWN.
THE NUMBER TO THE UPPER LEFT DESIGNATES THE BUTTON POSITION.
Figure 6. KEYBOARD DIAGRAM (Continued)

United States Keyboard Diagram



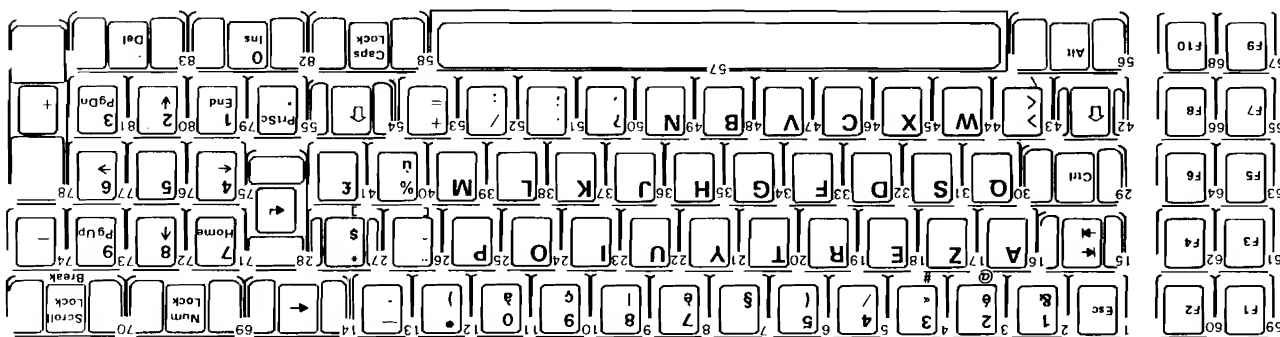
NOTE
1 NOMENCLATURE IS ON BOTH TOP AND FRONT FACE OF KEYBUTTON AS SHOWN.
THE NUMBER TO THE UPPER LEFT DESIGNATES THE BUTTON POSITION.
Figure 6. KEYBOARD DIAGRAM

NOTE
1 NOMENCLATURE IS ON BOTH TOP AND FRONT FACE OF KEYBUTTON AS SHOWN.
THE NUMBER TO THE UPPER LEFT DESIGNATES THE BUTTON POSITION.



German Keyboard Diagram

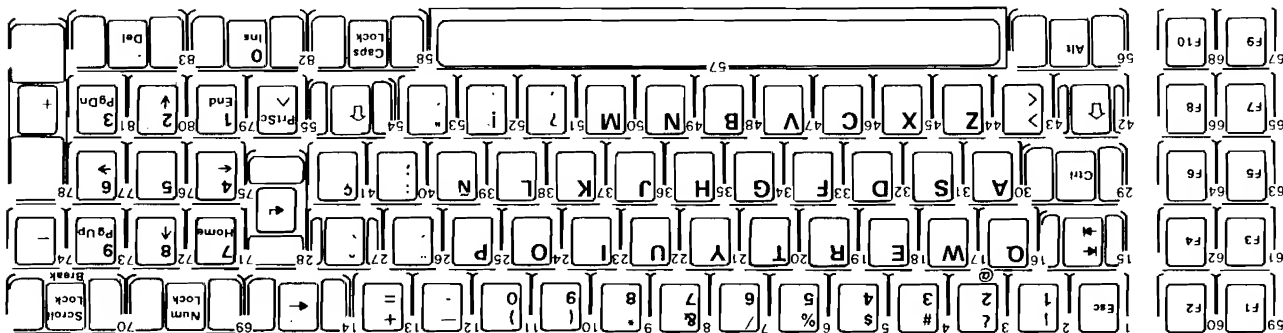
NOTE
1 NOMENCLATURE IS ON BOTH TOP AND FRONT FACE OF KEYBUTTON AS SHOWN. THE NUMBER TO THE UPPER LEFT DESIGNATES THE BUTTON POSITION.



French Keyboard Diagram

Figure 6. KEYBOARD DIAGRAM (Continued)

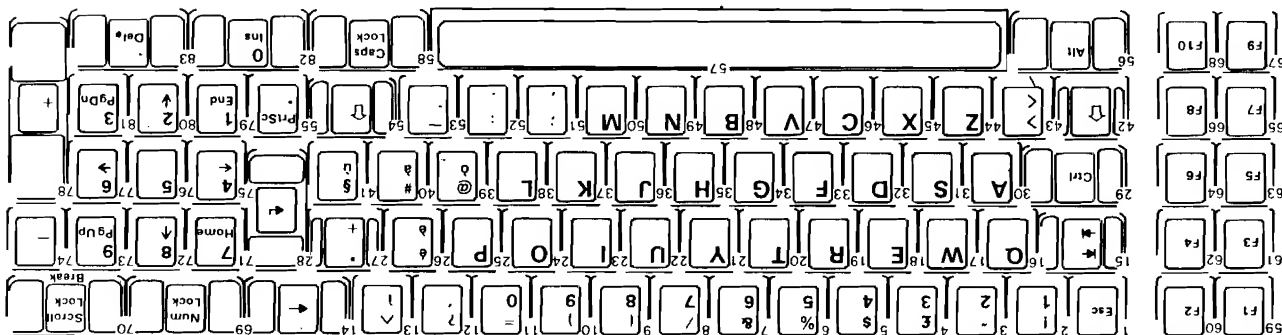
NOTE
1 NOMENCLATURE IS ON BOTH TOP AND FRONT FACE OF KEYBUTTON AS SHOWN.
THE NUMBER TO THE UPPER LEFT DESIGNATES THE BUTTON POSITION.



Spanish Keyboard Diagram

Figure 6. KEYBOARD DIAGRAM (Continued)

NOTE
1 NOMENCLATURE IS ON BOTH TOP AND FRONT FACE OF KEYBUTTON AS SHOWN.
THE NUMBER TO THE UPPER LEFT DESIGNATES THE BUTTON POSITION.

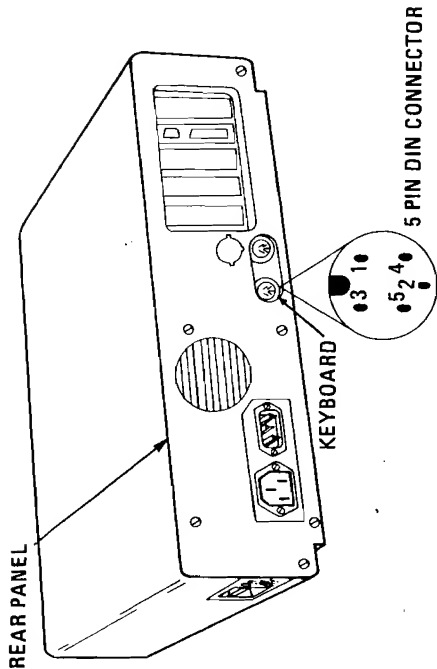


Italian Keyboard Diagram

Table 1. Keyboard Scan Codes

Key Position	Scan Code in Hex	Key Position	Scan Code in Hex
1	01	43	2B
2	02	44	2C
3	03	45	2D
4	04	46	2E
5	05	47	2F
6	06	48	30
7	07	49	31
8	08	50	32
9	09	51	33
10	0A	52	34
11	0B	53	35
12	0C	54	36
13	0D	55	37
14	0E	56	38
15	0F	57	39
16	10	58	3A
17	11	59	3B
18	12	60	3C
19	13	61	3D
20	14	62	3E
21	15	63	3F
22	16	64	40
23	17	65	41
24	18	66	42
25	19	67	43
26	1A	68	44
27	1B	69	45
28	1C	70	46
29	1D	71	47
30	1E	72	48
31	1F	73	49
32	20	74	4A
33	21	75	4B
34	22	76	4C
35	23	77	4D
36	24	78	4E
37	25	79	4F
38	26	80	50
39	27	81	51
40	28	82	52
41	29	83	53
42	2A		

Keyboard Interface Connector Specifications



PIN	SIGNAL
1	+ Keyboard Clock
2	+ Keyboard Data
3	- Keyboard Reset (Not used by keyboard)
4	Ground
5	+5 Volts

Cassette User Interface

The cassette interface control is implemented in software. (See FIRMWARE Section). An 8253 timer output is used to control the data to the cassette recorder. This output exits the System Board, at the rear, through pin 5 of a DIN connector. The cassette input data is read by an 8255A-5 Programmable Peripheral Interface (PPI) input port bit. This signal is received through pin 4 of the cassette connector. Software algorithms are used to generate and read cassette data. The cassette drive motor is controlled through pins 1 & 3 of the cassette connector. The motor on/off is controlled by an 8255A-PPI output port bit. (Port '61H', bit 3). The 8255A address and bit assignments are defined in the I/O Address Map page. On the following pages are read, write, and motor control block diagrams.

Cassette Jumpers

A 2x2 Berg Pin and Jumper are used on the cassette Data Out line. The jumper will allow the Data Out line to be used as a microphone input (75 mv.) when the jumper is placed across M and C pins. An auxiliary input is available when the jumper is placed across the A and C pins. The auxiliary input provides a .68 volt input to the recorder. Refer to System Board Component Diagram page (2-13) for cassette jumper location.



Circuit Block Diagrams

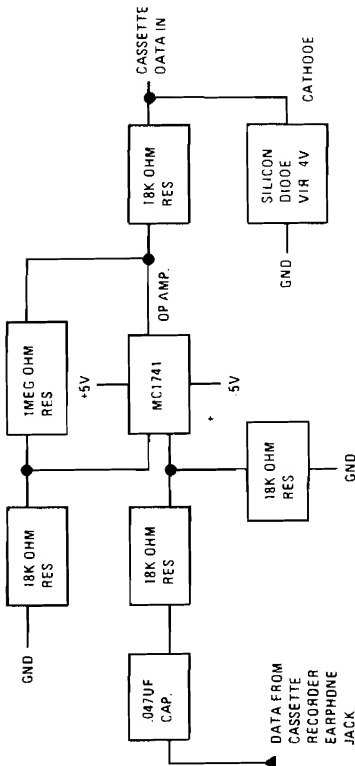
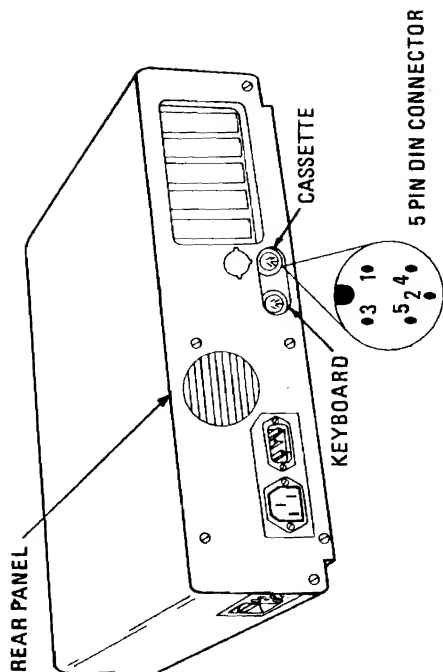


Figure 7. CASSETTE INTERFACE READ HARDWARE

Cassette Interface Connector Specifications



PIN	SIGNAL	ELECTRICAL CHARACTERISTICS*
1	Motor Control	Common from Relay
2	Ground	
3	Motor Control	6 VDC; 1A (Relay N.O.)
4	Data In	500nA at $\pm 13V$ - at 1,000 - 2,000 Baud
5	Data Out (Mic or Aux)	250 μA at $\left. \begin{array}{l} .68V \\ \text{or} \\ 75mV \end{array} \right\}$ **

*All voltages and currents are maximum ratings and should not be exceeded.

**Data out can be chosen using a jumper located on planar.
(AUX \rightarrow .68V or MIC \rightarrow 75 mV).

Interchange of these voltages on the cassette recorder could lead to damage of recorder inputs.

Figure 8. CASSETTE INTERFACE WRITE HARDWARE

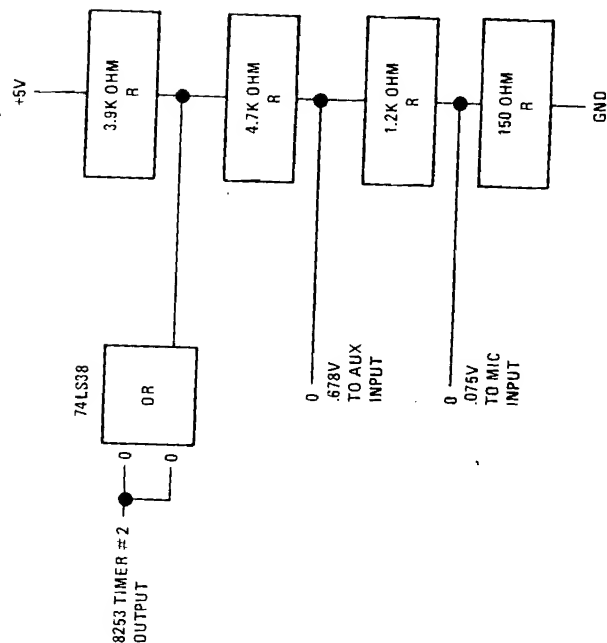
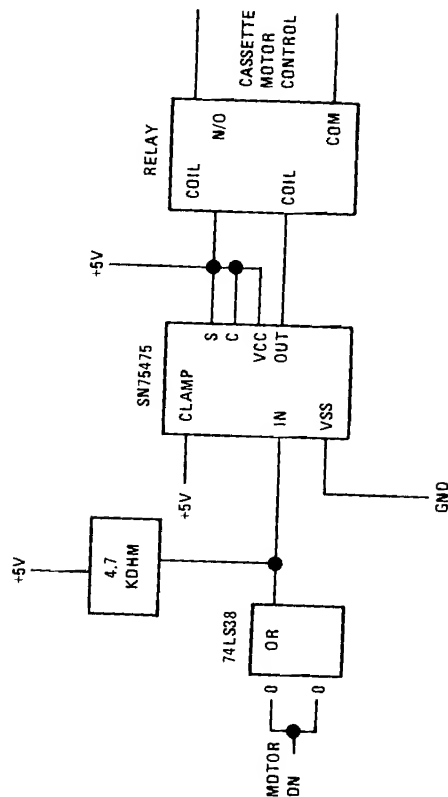


Figure 9. CASSETTE MOTOR CONTROL



Speaker Interface

The sound system contains a small permanent magnet 2-1/4" speaker. The speaker can be driven from one or both of two sources. The sources are:

1. An 8255A-5 PPI output bit. The address and bit are defined in the I/O Address Map pages 2-23 and 2-24.
2. A timer Channel Clock out where the output is programmable within the functions of the 8253-5 timer with a 1.19 Mhz clock input. The timer gate is also controlled by an 8255A-5 PPI output port bit. Address and bit assignment are in the I/O Address Map pages 2-23 and 2-24.

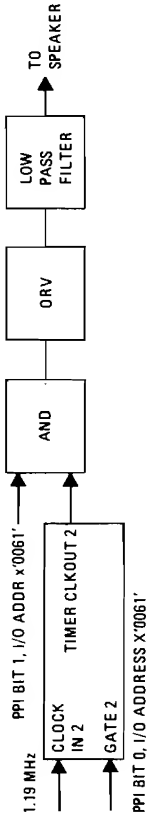


Figure 10. SPEAKER DRIVE SYSTEM BLOCK DIAGRAM

Channel 2 (Tone generation for Speaker)

GATE 2 — Controlled by 8255A-5 PPI Bit
(See I/O Map)

CLK IN 2 — 1.19318 Mhz OSC

CLK OUT 2 — Used to drive Speaker

— Used to write data on the Audio
Cassette

Speaker Connection - 4 Pin Berg Connector, Refer to
System Board Diagram page 2-13 for speaker connection.

PIN	FUNCTION
1	DATA
2	KEY
3	GROUND
4	+5 VOLTS

I/O Address Map

HEX RANGE	9	8	7	6	5	4	3	2	1	0	DEVICE
00-0F	0	0	0	0	0	Z	A3	A2	A1	A0	DMA CHIP 8237-2
20-2F	0	0	0	0	1	Z	Z	Z	Z	A0	INTERRUPT 8259A
40-4F	0	0	0	1	0	Z	Z	Z	A1	A0	TIMER 8253-5
60-6F	0	0	0	1	1	Z	Z	Z	A1	A0	PPI 8255A-5
80-8F	0	0	1	0	0	Z	Z	Z	A1	A0	DMA PAGE REGS
*4X	0	0	1	0	1	0					NMI MASK REG
CX	0	0	1	1	0						RESERVED
EX	0	0	1	1	1						RESERVED
200-20F	0	0	0	0	0	0	A3	A2	A1	A0	GAME I/O ADAPTER
278-27F	1	0	0	1	1	1	1	Z	A1	A0	RESERVED
2F8-2FF	1	0	1	1	1	1	1	A2	A1	A0	ALT RS232 CARD
300-31F	1	1	0	0	0	A4	A3	A2	A1	A0	PROTOTYPE CARD
378-37F	1	1	0	1	1	1	1	Z	A1	A0	PARALLEL PRINTER PORT
280-38F	1	1	1	0	1	1	A3	A2	A1	A0	IBM MONOCHROME DISPLAY// PARALLEL PRINTER ADAPTER
300-3DF	1	1	1	1	0	1	A3	A2	A1	A0	COLOR/GRAPHICS ADAPTER
3F0-3F7	1	1	1	1	1	1	0	A2	A1	A0	5-1/4" DRIVE ADAPTER
3F8-3FF	1	1	1	1	1	1	1	A2	A1	A0	TP RS232 CARD

Z = Don't Care, i.e., Not in Decode

* At power on time, the Non Mask Interrupt NMI into the 8088 is masked off. This mask bit can be set and reset via system software as follows:

Set mask: write X'80' to I/O Address X'A0' (enable NMI)

Clear mask: write X'00' to I/O Address X'A0' (disable NMI)

I/O Address Map

X'0060'	PA0	1	+K80 SCAN CODE	0	IPL 5 1/4 DISKETTE DRIVE RESERVED	(SW1-1)
	P	2		1	SYS. 80. READ/WRITE MEMORY SIZE	(SW1-2)
	N	3		2	SYS. 80. READ/WRITE MEMORY SIZE	(SW1-3)
	P	4		3	+DISPLAY TYPE 1	(SW1-4)
	U	5		4	+DISPLAY TYPE 2	(SW1-5)
	T	6		5	NO. OF 5 1/4 DRVS	(SW1-6)
		7		6	NO. OF 5 1/4 DRVS	(SW1-7)
				7		(SW1-8)
X'0061'	PB0	1	+TIMER 2 GATE SPEAKER			
	U	2	+SPEAKER DATA			
	T	3	+READ/READ/WRITE MEMORY SIZE) OR (READ SPARE KEY)			
	P	4	+CASSETTE MOTOR OFF			
	U	5	-ENABLE READ/WRITE MEMORY			
	U	6	-ENABLE I/O CH CK			
	T	7	-HOLD K80 CLK LOW			
			-(ENABLE K80) OR + (CLR K80 & ENABLE SENSE SW'S)			
X'0062'	PC0	1	I/O READ/WRITE MEMORY (SW2-1)		BINARY	OR SPARE KEY (SW2-5)
	N	2	I/O READ/WRITE MEMORY (SW2-2)		VALUE	
	P	3	I/O READ/WRITE MEMORY (SW2-3)		X 32KB	
	U	4	+CASSETTE DATA IN			
	U	5	+TIMER CHANNEL 2 OUT			
	T	6	+I/O CHANNEL CHECK			
		7	+READ/WRITE MEMORY PCK			
X'0063'	CNO/MODE REGISTER					
		7				
		6				
		5				
		4				
		3				
		2				
		1				

MODE REG VALUE	7	6	5	4	3	2	1	0
	1	0	0	1	1	0	0	1

•	PA3	SW1-4	PA2	SW1-3	AMOUNT OF MEMORY LOCATED ON SYS. 80.
	0	0	0	0	18K BYTES
	0	1	1	1	32K BYTES
	1	0	0	0	48K BYTES
	1	1	1	1	64K BYTES
	PA5	SW1-6	PA4	SW1-5	TYPE OF DISPLAY
	0	0	0	0	RESERVED
	0	1	1	1	COLOR CARD 40X25 (BW MODE)
•••	PA7	SW1-8	PA6	SW1-7	COLOR CARD 80X25 (BW MODE)
	0	0	0	0	18M MONOCHROME DISPLAY (80 X 25)
	0	1	1	1	NUMBER OF 5-1/4" DRIVES IN SYSTEM
	1	0	0	0	1
	1	0	1	1	2
	1	1	0	0	3
	1	1	1	1	4
					8255A - I/O BIT MAP

NOTE: PA bit=0 implies switch "ON".
PA bit=1 implies switch "OFF".

System Memory Map

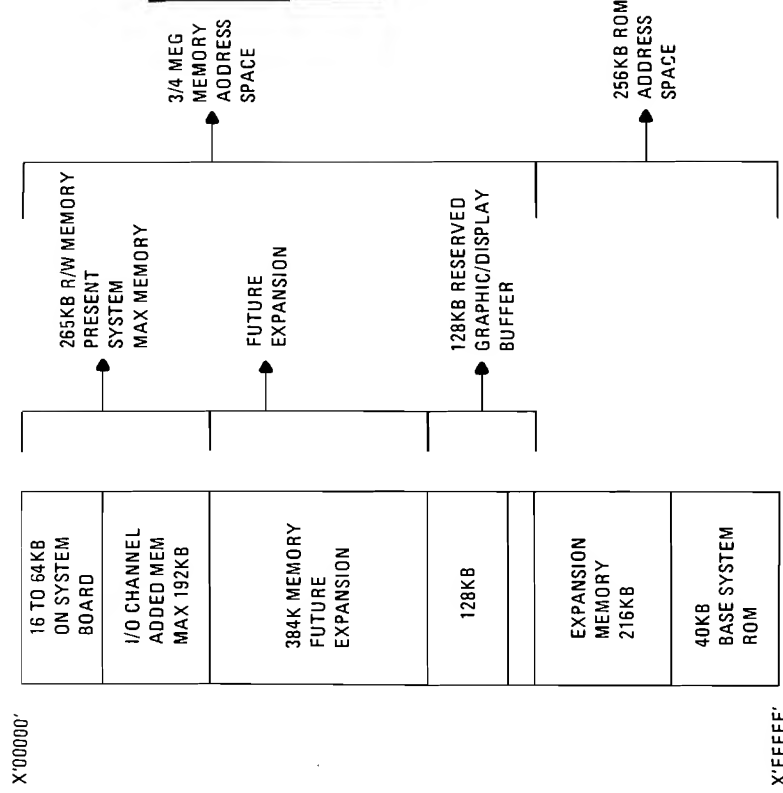


Figure 11. SYSTEM MEMORY MAP

System Memory Map (Increments of 16KB)

START ADDRESS: DECIMAL HEX	FUNCTION:
0 16K 32K 48K	16-64 KB READ/WRITE MEMORY ON SYSTEM BOARD
64K 80K 96K 112K	
128K 144K 160K 178K	
192K 208K 224K 240K	
256K 272K 288K 304K	UP TO 192 KB MEMORY IN I/O CHANNEL
320K 336K 352K 368K	
384K 400K 416K 432K	
448K 464K 480K 496K	
512K 528K 544K 560K	384 KB FUTURE R/W MEMORY EXPANSION IN I/O CHANNEL
576K 592K 608K 624K	
640K 656K 672K 688K	
704K 720K 736K 752K	
768K 784K 800K 816K	112 KB GRAPHICS/DISPLAY VIDEO BUFFER
832K 848K 864K 880K	
896K 912K 928K 944K	
960K 976K 992K 1,008M	

Figure 12. SYSTEM MEMORY MAP (INCREMENTS OF 16KB) (SHEET 1 OF 2)

System Memory Map Cont.

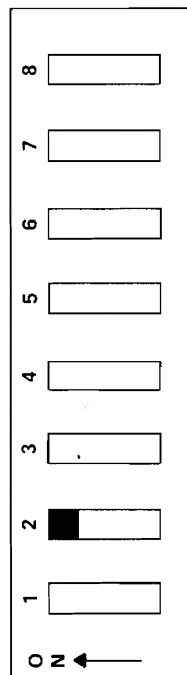
START ADDRESS: DECIMAL HEX	FUNCTION:
640K 656K 672K 688K	RESERVED
704K 720K 736K 752K	
768K 784K 800K 816K	
832K 848K 864K 880K	
896K 912K 928K 944K	192 KB MEMORY EXPANSION AREA
960K 976K 992K 1,008M	
1024K 1040K 1056K 1072K	
1088K 1104K 1120K 1136K	

Figure 12. SYSTEM MEMORY MAP (16KB) (SHEET 2)

System Board and Memory Expansion Switch Settings

On the following four pages are graphic illustrations of switch settings. These are necessary for the system to address components attached, and to specify the amount of memory installed both on the System Board and in the System Expansion Slots. Refer to the System Board Component Diagram (page 2-13) for DIP switch locations.

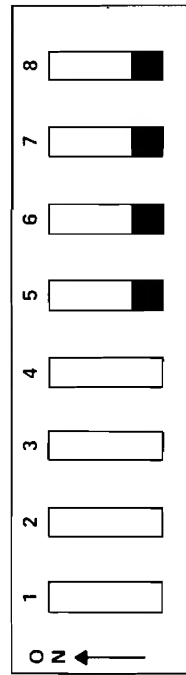
SWITCH 1



Position Function

- 1-7-8 Number of 5-1/4" Diskette Drives Installed; page 2-29
- 2 Unused — must be on (reserved for co-processor)
- 3-4 Amount of memory on System Board; pages 2-30 to 2-31
- 5-6 Type of monitor you are using; page 2-29

SWITCH 2

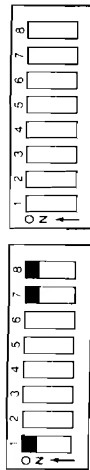


Position Function

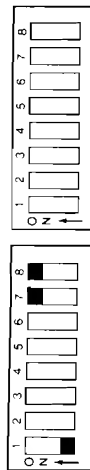
- 1-2-3-4 Amount of memory options installed; page 2-30 to 2-31
- 5-6-7-8 Always in the OFF position

Number of 5-1/4" Diskette Drives Installed

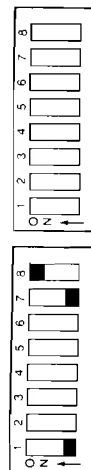
SWITCH 1 SWITCH 2



0—Drives



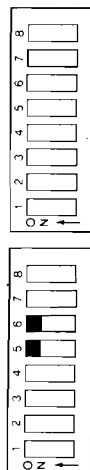
1—Drive



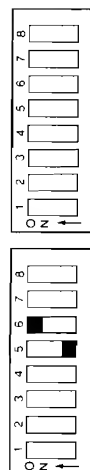
2—Drives

Monitor Type

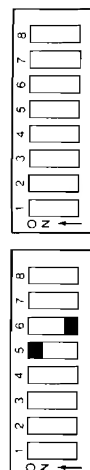
SWITCH 1 SWITCH 2



No Monitors

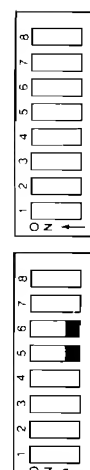


40 x 25 Color



80 x 25 Color

Note: The 80 x 25 color setting, when used with home television and various monitors can cause loss of character/quality.



IBM Monochrome Display or more than one monitor

System Board Memory Switch Settings

Total Memory	Switch 1	Switch 2
16KB		
32KB		
48KB		
64KB		
96KB		
128KB		
160KB		
192KB		
224KB		
256KB		

SYSTEM BOARD

System Board Memory Switch Settings

Total Memory	Switch 1	Switch 2
288KB		
320KB		
352KB		
384KB		
416KB		
448KB		
480KB		
512KB		
544KB		

MEMORY OPTIONS

Memory Expansion Options

The following are switch settings on each Memory Expansion Option.

Total Memory	Option 1	Option 2	Option 3
96KB			
128KB			
128KB			
128KB			
160KB			
160KB			
160KB			

*Amount of memory installed on a 64/256KB Memory Expansion Option.

Memory Expansion Options

The following are switch settings on each Memory Expansion Option.

Total Memory	Option 1	Option 2	Option 3
192KB			
192KB			
192KB			
192KB			
192KB			
224KB			
224KB			
224KB			

*Amount of memory installed on a 64/256KB Memory Expansion Option.

Memory Expansion Options

The following are switch settings on each Memory Expansion Option.

Total Memory	Option 1	Option 2	Option 3
256KB	192KB*	64KB	64KB
256KB	128KB*	64KB	64KB
256KB	64KB*	64KB	32KB
256KB	64KB	64KB	32KB
256KB	128KB*	32KB	32KB
288KB	192KB*	32KB	32KB
288KB	128KB*	64KB	32KB
320KB	128KB*	64KB	64KB

*Amount of memory installed on a 64/256KB Memory Expansion Option.

Memory Expansion Options

The following are switch settings on each Memory Expansion Option.

Total Memory	Option 1	Option 2	Option 3
320KB	192KB*	64KB	32KB
320KB	192KB*	32KB	32KB
320KB	256KB*		
352KB	192KB*	64KB	32KB
352KB	256KB*	32KB	
384KB	192KB*	64KB	64KB
384KB	256KB*	64KB*	
384KB	256KB*	64KB	
384KB	256KB*	32KB	32KB

*Amount of memory installed on a 64/256KB Memory Expansion Option.

Memory Expansion Options

The following are switch settings on each Memory Expansion Option.

Total Memory	Option 1 256KB*	Option 2 64KB*	Option 3 32KB
416KB			
416KB			
448KB			
448KB			
448KB			
480KB			
512KB			
512KB			
544KB			

*Amount of memory installed on a 64/256KB Memory Expansion Option.

Power Supply

The system DC power supply is a 63.5 watt, 4 voltage level switching regulator. It is integrated into the System Unit and supplies power for the System Unit, its options, and the keyboard. The supply provides 7 amps of +5 Vdc, $\pm 5\%$ 2 amps of +12 Vdc, $\pm 5\%$ 300 ma of -5 Vdc, $\pm 10\%$ and 250 ma of -12 Vdc, $\pm 10\%$. All power levels are regulated with overvoltage and over current protection. If DC over-load or over-voltage conditions exist, the supply will automatically shut down until the condition is corrected. The supply is designed for continuous operation at 63.5 watts and the input to the supply is fused.

There are two different power supplies available for the system unit: one that has an input voltage of 120 Vac and one that has an input voltage of 220/240 Vac. Other than their input ratings the two power supplies have identical specifications.

The System Board takes approximately 3 amps of +5 Vdc thus allowing approximately 4 amps of 5 Vdc for the adapters in the System Expansion Slots. The +12 Vdc power level is designed to power the two internal 5-1/4" Diskette Drives and the system's dynamic memory. It is assumed that only one drive motor is active at a time. The -5 Vdc level is used for memory bias voltage and analog circuits in the diskette adapter phase lock loop. The +12 Vdc and -12 Vdc are used for powering the serial interface card EIA drivers and receivers for the Asynchronous Communications Adapter. All four power levels are bussed across the five System Expansion Slots and available for option adapter.

The IBM Monochrome Display has its own power supply. This high resolution display receives its AC power from the System Unit power supply and is switched on and off with the power switch, which saves a wall outlet. The AC output for the display is a nonstandard connector, so only the AC high resolution Display can use this AC port.

Power Supply Location

The Power Supply is located at the right rear area of the System Unit. It supplies operating voltages to the System Board, IBM Monochrome Display, and provides two separate connections for power to the 5-1/4" Diskette Drives (if installed). The nominal power requirements and output voltages are listed on the following tables:

Input Requirements 120 Volt

VOLTAGE Vac		FREQUENCY Hz	CURRENT MAX
NOMINAL	MINIMUM	MAXIMUM	@V _{in} MINIMUM
120	104	± 3 Hz 60	2.5 AMPS @ 104 Vac

Input Requirements 220/240 Volt

VOLTAGE Vac		FREQUENCY Hz	CURRENT MAX
NOMINAL	MINIMUM	MAXIMUM	@V _{in} MINIMUM
220/240	180	± 3 Hz 50	1.0 AMPS @ 180 Vac

DC Output

VOLTAGE V _{dc}	CURRENT AMPS		REGULATION TOLERANCE	
NOMINAL	MIN	MAX	± %	- %
+ 5.0	2.3	7.0	5	4
- 5.0	0.0	0.3	10	8
+12.0	0.0	2.0	5	4
-12.0	0.0	0.25	10	9

AC Output

The AC voltage out is connected to the input voltage through the power supply fuse filter card and On/Off switch. Since this output is designed to support only the IBM Monochrome Display and since the supply input is fused, there is only a limited amount of current available: .75 A maximum on the 120 Vac supply and .38 A maximum on the 220/240 Vac power supply.

Power Supply Connectors and Pin Assignment

The power connector on the System Board is a 12 pin male connector which plugs into the power supply connectors. The pin configurations and locations are shown below:

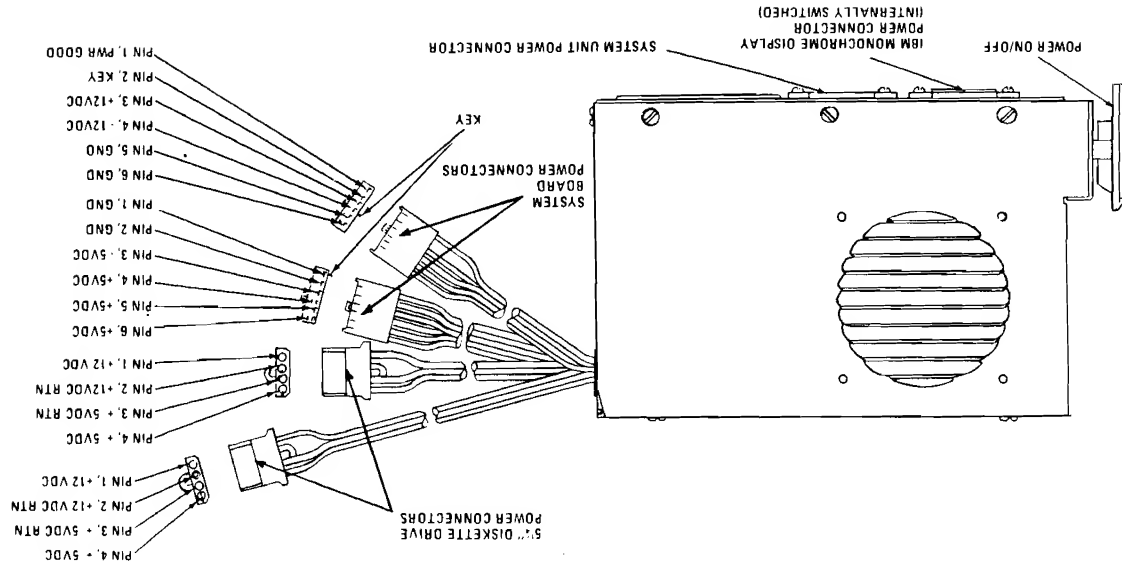


Figure 13. POWER SUPPLY AND CONNECTORS

IBM Monochrome Display and Parallel Printer Adapter

Important Operating Characteristics

Over Voltage/Current Protection

PRIMARY (INPUT)

VOLTAGE NOMINAL VAC	TYPE PROTECTION	RATING AMPS
120	60 Hz FUSE TYPE 2 SOC SD4	2 AMPS
240	50 Hz FUSE TYPE 2 SOC SD4	1 AMP

Power On/Off Cycle: When the supply is turned off for a minimum of 5 seconds, and then turned on, the power good signal will be regenerated.

Signal Requirements

The power good signal indicates that there is adequate power to continue processing. If the power goes below the specified levels, the power good signal triggers a system shut-down.

The Power Supply provides a power good signal out, to indicate that the +/-5V and +/-12V outputs are above the sense level defined in the chart below. The power good signal is up level (2.4V to 5.5V), TTL compatible, and capable of sourcing 60 UA. When any of the four sensed output voltages is below its sense level voltage as defined in the chart below, the power good signal is down level (0V to 0.4V), TTL compatible, and capable of sinking 500 UA. The power good signal (after all levels of the output voltage are good) has a turn on delay of at least 100 MS but no more than 500 MS.

The sense levels of the +/-5V and +/-12V outputs are :

OUTPUT	MIN	SENSE VOLTAGE NOMINAL	MAX
+5V	+3.7	+4.0	+4.3
-5V	-3.7	-4.0	-4.3
+12V	+8.5	+9.6	+10.5
-12V	-8.5	-9.6	-10.5

This adapter has dual functions. The first is to provide the interface to the IBM Monochrome Display. The second function is a parallel interface for the IBM 80 CPS Matrix Printer.

The monitor interface is designed around the Motorola 6845 CRT Controller module. There are 4K bytes of static memory on the card which are used for the display buffer. The memory is dual ported and may be accessed directly by the CPU. No parity is provided on the display buffer. A block diagram of the Monochrome Display function in on page 2-48.

The characteristics of the design are listed below:

- 80x25 Screen
- Direct Drive Output
- 9x14 Character Box
- 7x9 Character
- 18 Khz Monitor
- Character Attributes

The adapter supports 256 character codes. An 8K byte character generator contains the fonts for the character codes. The characters, values, keystrokes and screen characteristics are tabled in Appendix C. Of Characters, Keystrokes and Color.

Note: This Adapter when used with a display containing P39 Phosphor, will not support a light pen!

Parallel Interface Description

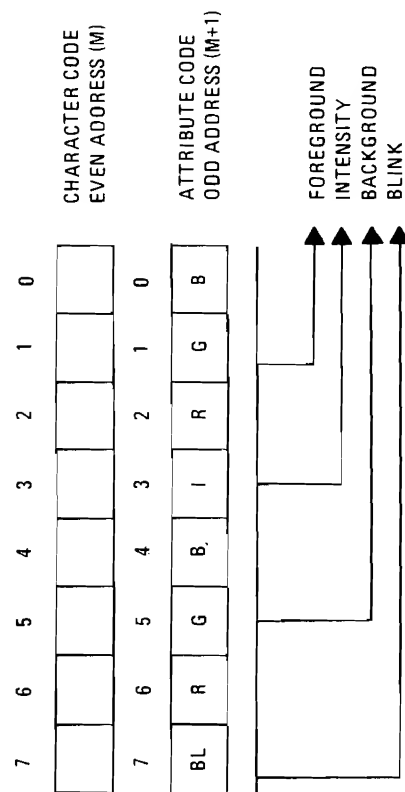
This topic is discussed in full on pages 2-75 through 2-79.

System Channel Interface

Figure 14. IBM Monochrome Display Adapter Block Diagram

Modes of Operation

The IBM Monochrome Display and Printer Adapter supports 256 character codes. In the character set are alphanumerics and block graphics. Each character in the display buffer has a corresponding character attribute. The character code must be an even address and the attribute code must be an odd address in the display buffer.



The adapter decodes the character attribute byte as defined above. The BLINK and INTENSITY bits may be combined with the FOREGROUND and BACKGROUND bits to further enhance the character attribute functions listed below.

BACKGROUND R G B	FOREGROUND R G B	FUNCTION
0 0 0	0 0 0	NON DISPLAY
0 0 0	0 0 1	UNDERLINE
0 0 0	1 1 1	WHITE CHARACTER/ BLACK BACKGROUND
1 1 1	0 0 0	REVERSE VIDEO

Programming Considerations

Programming the 6845 CRT Controller

The following table summarizes the 6845 Internal Data Registers and their functions and parameters. For the IBM Monochrome Display, the values in the table must be programmed into the 6845 to insure proper initialization of the device.

Table 2. 6845 Initialization Parameters

REGISTER =	REGISTER FILE	PROGRAM UNIT	80x25 MONOCHROME
R0	HORIZONTAL TOTAL	CHARACTERS	61H
R1	HORIZONTAL DISPLAYED	CHARACTERS	50H
R2	HSYNC POSITION	CHARACTERS	52H
R3	HSYNC WIDTH	CHARACTERS	FH
R4	VERTICAL TOTAL	CHAR ROWS	19H
R5	VERTICAL ADJUST	SCAN LINE	6H
R6	VERTICAL DISPLAYED	CHAR ROW	19H
R7	VSYNC POSITION	CHAR ROW	19H
R8	INTERLACE MODE	---	02
R9	MAX SCAN LINE ADDRESS	SCAN LINE	DH
R10	CURSOR START	SCAN LINE	8H
R11	CURSOR END	SCAN LINE	CH
R12	START ADDRESS (H)	---	00H
R13	START ADDRESS (L)	---	00H
R14	CURSOR (H)	---	00H
R15	CURSOR (L)	---	00H
R16	RESERVED	---	---
R17	RESERVED	---	---

Sequence of Events

The first command issued to this attachment must be to output to PORT 3B8, hex 01, to set high resolution mode. If the high resolution mode is not set, an infinite CPU wait-state will occur!

Memory Requirements

The attachment has 4K bytes of memory which is used for the display buffer. The memory supports one screen of 25 rows of 80 characters, plus a character attribute for each display character. No parity is provided on the memory. No system Read/Write memory is required for the monochrome adapter portion. The display buffer starts at address 'B0000'.

DMA Channels

The display buffer will support a DMA operation, however CPU wait-states will be inserted during DMA.

Interrupt Levels

Interrupt Level 7 is used on the parallel interface. Interrupts can be enabled or disabled via the Printer Control Port. The interrupt is a high level active signal.

I/O Address and Bit Map

The table below breaks down the functions of the I/O Address decode for the card. The I/O address decode is from '3B0' through '3BF'. The bit assignment for each I/O address follows:

I/O Address Function

3B0	Not Used
3B1	Not Used
3B2	Not Used
3B3	Not Used
3B4	6845 Index Register
3B5	6845 Data Register
3B6	Not Used
3B7	Not Used
3B8	CRT Control Port 1
3B9	Reserved
3BA	CRT Status Port
3BB	Reserved
3BC	Parallel Data Port
3BD	Printer Status Port
3BE	Printer Control Port
3BF	Not Used

The 6845 Index and Data Registers are used to program the CRT controller to interface to the high resolution Monochrome Display.

- CRT Output Port 1 (I/O Address '3B8')

Bit #	Function
0	+ high resolution mode
1	Not Used
2	Not Used
3	+ video enable
4	Not Used
5	+ enable blink
6, 7	Not Used

- CRT Status Port (I/O Address '3BA')

Bit #	Function
0	+ horizontal Drive
1	Reserved
2	Reserved
3	+ B/W Video

IBM Monochrome Display

The high resolution IBM Monochrome Display unit attaches to the System Unit via two cables of approximately 3' (914 mm) in length. One cable is a signal cable which contains direct drive interface from the IBM Monochrome Display and Printer Adapter. The second cable provides AC power to the display from the System Unit. This allows the System Unit power On/Off switch to also control the display unit. An additional benefit is a reduction in the requirements for wall outlets to power the system. The monitor contains an 11.5" (283.1 mm) diagonal 90° deflection CRT. The CRT and analog circuits are packaged in an enclosure so the display may either sit on top of the System Unit or on a nearby table top or desk. The unit has both brightness and contrast adjustment controls on the front available to the operator.

Operating Characteristics

Screen

High persistence green phosphor (P 39) with an etched surface to reduce glare. Unit displays an 80 character by 25 line screen with a 9 dot wide by 14 dot tall character box.

Video Signal

Maximum video bandwidth of 16.27 Mhz.

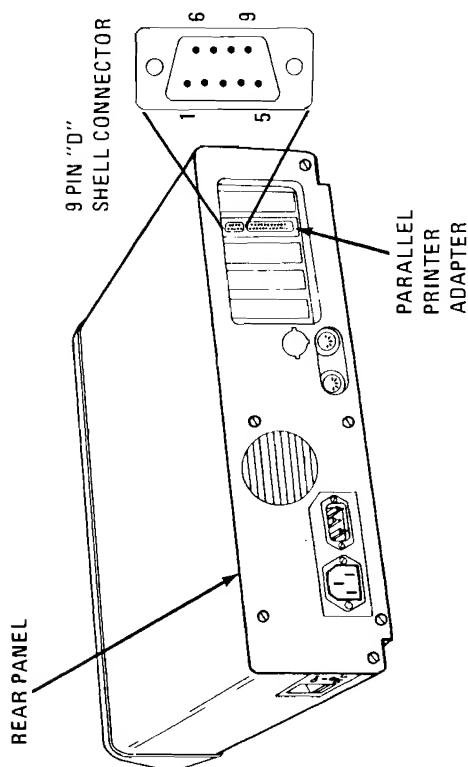
Vertical Drive

Screen refreshed at 50 Hz with 350 vertical lines of resolution and 720 lines of horizontal resolution measured at center of screen.

Horizontal Drive

Positive level TTL compatible frequency, 18.432 KHz.

IBM Monochrome Direct Drive Interface and Pin Assignment



At Standard TTL Levels

IBM Monochrome Display	At Standard TTL Levels								
	1	2	3	4	5	6	7	8	9
	Ground	Ground	Not Used	Not Used	Not Used	+ Intensity	+ Video	+ Horizontal	- Vertical

NOTE: Signal voltages are 0 - .6 Vdc at down level
+5 Vdc at high level

Color/Graphics Monitor Adapter

The Color/Graphics Monitor Adapter is designed to attach a wide variety of NTSC (U.S. National Television System Committee) standard TV frequency monitors and TV sets (user-supplied RF modulator required for TVs). It is capable of operating in black and white or color, and provides three video interfaces: a composite video port, a direct drive port, and a connection interface for driving a user supplied RF modulator. In addition, a light pen interface is provided.

The adapter has two basic modes of operation; alphanumeric (A/N) and all points addressable graphics (APA). Additional modes are available within A/N and APA modes. In A/N mode, the display can be operated in a 40x25 mode for low resolution monitors and TVs or 80x25 mode for high resolution monitors. In both modes, characters are defined in an 8x8 box and are 7x7 with one line of descender for lowercase (both uppercase and lowercase characters are supported in all modes). In black and white mode, the character attributes of Reverse Video, Blinking and High-lighting are available. In color mode, there are 16 foreground colors and 8 background colors available per character. In addition, blinking on a per character basis is available.

The adapter card contains 16KB of storage; thus, for a 40x25 screen, 1000 bytes are used to store character information and 1000 bytes are used for attribute/color information. This means that up to 8 pages of screens can be stored in the adapter memory. Similarly, in an 80x25 mode, 4 pages of display screen may be stored in the adapter. The full 16KB storage on the display adapter is directly addressable by the processor allowing maximum software flexibility in managing the screen. In A/N color modes, it is also possible to select the screen border color. One of 16 colors may be selected.

In APA mode, there are two resolutions available; 320x200 and 640x200. In the 320x200, each (picture element) pel may have one of four colors. The background color (color 0) may be any of the 16 possible colors. The remaining 3 colors come from one of the two software selectable palettes. One palette contains red/green/brown, the other contains cyan/magenta/white.

The 640x200 mode is only available in black and white since the full 16KB of storage is used to define the on or off state of the pel. The adapter operates in noninterlace mode at either 7 or 14 megahertz (Mhz) video bandwidth depending on the mode of operation selected. Vertical scan output frequency is 60 Hz and horizontal output frequency is 15,750 Hz.

In A/N mode, characters are formed from a ROM character generator. The character generator contains dot patterns for 256 characters. The character set contains the following major grouping of characters. Sixteen special characters for game support, 15 characters for support of word processing editing functions, the standard 96 ASCII graphic set, 48 characters to support foreign languages, 48 characters for business block graphics allowing drawing of charts, boxes and tables using single and double lines, 16 of the most often used Greek characters, and 15 of the most often used scientific notation characters.

The Color/Graphics Monitor Adapter Function is packaged on a single card which fits into one of the five System Expansions Slots on the System Board. The direct drive and composite video ports are right-angle mounted connectors at the rear of the adapter and extend through the rear panel of the System Unit.

The display adapter is implemented using a Motorola 6845 CRT controller device. This adapter is highly programmable with respect to raster and character parameters. A block diagram of the Color/Graphics Adapter is on the following page.

HARDWARE

Color/Graphics Monitor Adapter Block Diagram

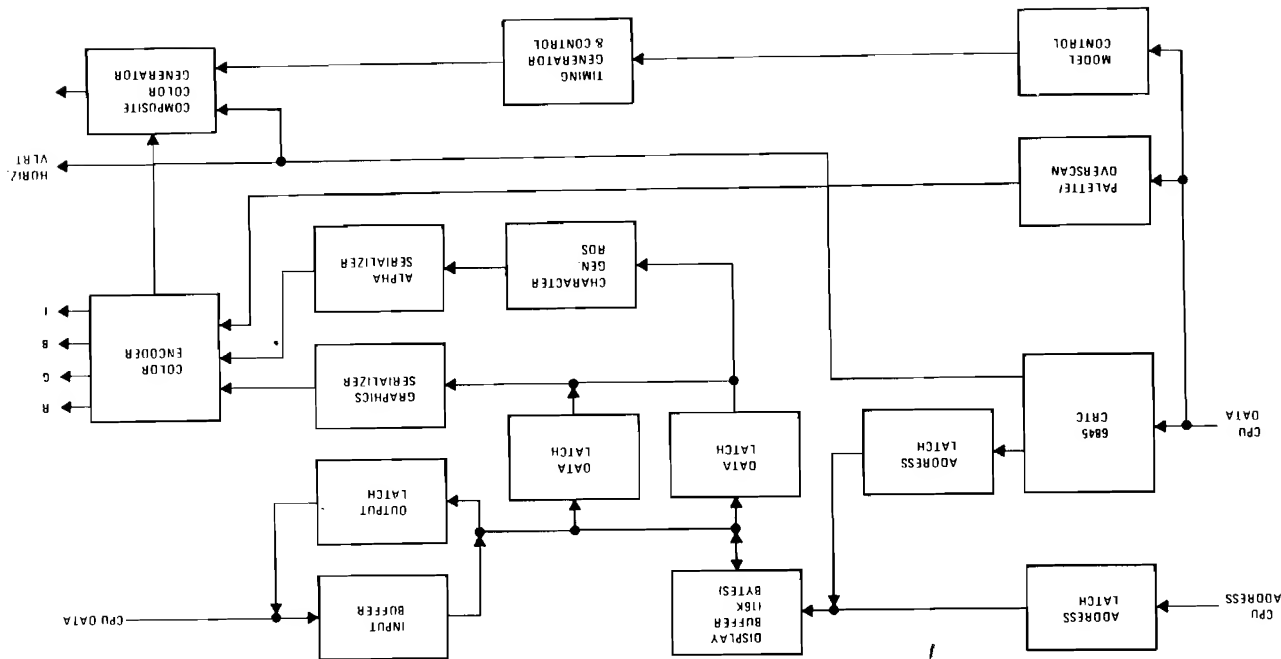


Figure 15. COLOR/GRAPHICS MONITOR ADAPTER BLOCK DIAGRAM

Major Components Definitions

Motorola 6845 CRT Controller

This device provides the necessary interface to drive a raster scan CRT.

Mode Set and Status Registers

This is a general purpose programmable I/O register. It has I/O points which may be individually programmed. Its function in this attachment is to provide mode selection (page 2-49 and 2-50) and color selection in the medium resolution color graphics mode (page 2-51).

Display Buffer

The Display Buffer resides in the CPU address space starting at address X'B8000'. It provides 16K bytes of dynamic read/write memory. A dual-ported implementation allows the CPU and the graphics control unit to access this buffer. The CPU and the CRT control unit have equal access to this buffer during all modes of operation except in high resolution alphanumeric mode. In this mode the CPU should access this buffer during the horizontal retrace intervals. The CPU may however, write to the required buffer at any time, but a small amount of display fetches will result if not during retrace intervals.

Character Generator

This attachment utilizes a ROM character generator. It consists of 8K bytes of storage which cannot be read/written under software control. This is a general purpose ROM character generator with three different character fonts. Two character fonts are used on this card (a 7x7 double dot and 5x7 single dot), selected by a card jumper. No jumper gives a 7x7 double dot; with a jumper a single dot font is selected.

Timing Generator

This block generates the timing signals used by the 6845 CRT controller and by the dynamic memory. It also resolves the CPU/graphic controller contentions for accessing the Display Buffer.

Composite Color Generator

The logic in this block generates base band video color information.

Modes of Operation

There are two basic modes of operation, 'Alphanumeric' and 'Graphics'. Each of these modes provide further options in both color and black-and-white. The following text describes each mode of operation.

Alphanumeric Mode

Alphanumeric Display Architecture

Every display character position is defined by two bytes in the regen buffer (part of display adapter, not system memory). Both the color and the black and white display adapter use this 2 byte character/attribute format.

DISPLAY CHAR CODE BYTE								ATTRIBUTE BYTE							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Attribute Byte Definition

ATTRIBUTE BYTE

ATTRIBUTE FUNCTION								ATTRIBUTE BYTE							
								7	6	5	4	3	2	1	0
NORMAL								B	R	G	B	I	R	G	B
REVERSE VIDEO								FG	BACKGROUND				FOREGROUND		
NON DISPLAY (BLK)								B	0	0	0	1	1	1	1
NON DISPLAY (WHITE)								B	1	1	1	1	1	1	1

I = HIGH LIGHT FOREGROUND (CHAR)

B = BLINK FOREGROUND (CHAR)

Color TV (NTSC - U.S. Standard)

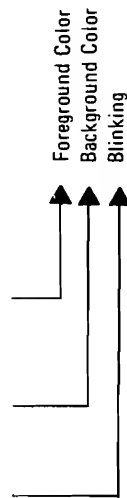
- Display up to 25 rows of 40 characters each
- Maximum of 256 characters
- Requires 2000 bytes of Read/Write Memory (on the adapter)
- 8x8 character box
- 7x7 double dotted characters (one descender)
- Character attributes (one for each character)

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
CHARACTER CODE								ATTRIBUTE CODE							
EVEN ADDRESS (M) ODD ADDRESS (M+1)															

ATTRIBUTE BYTE DEFINITIONS

R: Red
G: Green
B: Blue
I: Intensity

7	6	5	4	3	2	1	0
B	R	G	B	I	R	G	B



Note: The starting address of the display buffer must be an even location.

Color Monitor (with Drive input capability and 60 Hz vertical refresh)

Display up to 25 rows of 80 characters each

Requires 4000 bytes of Read/Write Memory (on the adapter)

Maximum of 256 character set

8x8 character box

7x7 character with one descender

Same format for attributes as for color TV

Note: The starting address of the display buffer must be an even location.

HARDWARE

IBM Monochrome Display Adapter Vs. Color/Graphics Adapter Attribute Relationship

Table 3. Monochrome Vs. Color/Graphics Attributes

ON THE MONOCHROME DISPLAY ADAPTER								ON THE COLOR/GRAPHIC DISPLAY ADAPTER							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
B	R	G	B	I	R	G	B	CHAR. COLOR	BKGD. COLOR	CHAR. COLOR	BKGD. COLOR	CHAR. COLOR	BKGD. COLOR	CHAR. COLOR	BKGD. COLOR
FG BACKGROUND								FG BACKGROUND							
B	0	0	0	1	1	1	1	WHITE	BLACK	WHITE	BLACK	WHITE	BLACK	WHITE	BLACK
R	1	1	1	1	0	0	0	BLACK	WHITE	BLACK	WHITE	BLACK	WHITE	BLACK	WHITE
G	0	0	0	1	0	0	0	BLACK	WHITE	BLACK	WHITE	BLACK	WHITE	BLACK	WHITE
B	1	1	1	1	1	1	1	WHITE	BLACK	WHITE	BLACK	WHITE	BLACK	WHITE	BLACK

NORMAL
RVV
NON DISP (BLK)
NON DISP (WHT)

ALL OTHER CODES
DEFINE FOREGROUND
BACKGROUND COLOR
COMBINATIONS

ALL OTHER
CODES RESULT
IN WHITE
CHAR ON BLACK
BACKGROUND

ALL OTHER
CODES CHANGE
FOREGROUND
BACKGROUND
COLOR TO
SELECTED
VALUE

R G B

CODE WRITTEN WITH AN UNDERLINE
ATTRIBUTE FOR THE IBM MONOCHROME DISPLAY
WHEN EXECUTED ON A COLOR/GRAPHICS ADAPTER
WILL RESULT IN A BLUE CHARACTER
WHERE THE UNDERLINE ATTRIBUTES
ARE ENCOUNTERED

CODE WRITTEN ON A COLOR/GRAPHICS ADAPTER
WITH BLUE CHARACTERS, WILL BE
DISPLAYED AS WHITE CHARACTERS
ON BLACK BACKGROUND WITH A
WHITE UNDERLINE ON THE MONOCHROME DISPLAY

* AN ADDITIONAL
8 COLOR (ACTUAL)
DIFFERENT SHADES
OF THE ABOVE
ARE SELECTED BY
SETTING THE
(I) BIT

Note: Not all Monitors Recognize the (I) Bit

Table 4. Color/Graphics Modes

	HORIZONTAL	VERTICAL	NO OF COLORS (INCL. BACKGROUND COLOR)
LOW RES	160	100	16 (INCLUDES BLACK AND WHITE)
MED RES	320	200	4 COLORS: 1 OF 16 FOR BACKGROUND PLUS GREEN, RED, YELLOW OR CYAN, MAGENTA, WHITE
HIGH RES	640	200	8 B & W ONLY

1. Low resolution color graphics (TV or monitor).
(Note: This mode is not supported in ROM).
 - Up to 100 rows of 160 pels each (2x2)
 - 1 of 16 colors each pel specified by I, R, G and B
 - Requires 8000 byte of Read/Write Memory (on the adapter)
 - Memory mapped graphics (requires special memory map and set up to be defined later)
2. Medium resolution color graphics (TV or monitor)
 - Up to 200 rows of 320 pels each (1x1)
 - 1 out of 4 preselected colors in each box
 - Requires 16000 bytes of Read/Write Memory (on the adapter)
 - Memory mapped graphics
 - 4 pels/byte

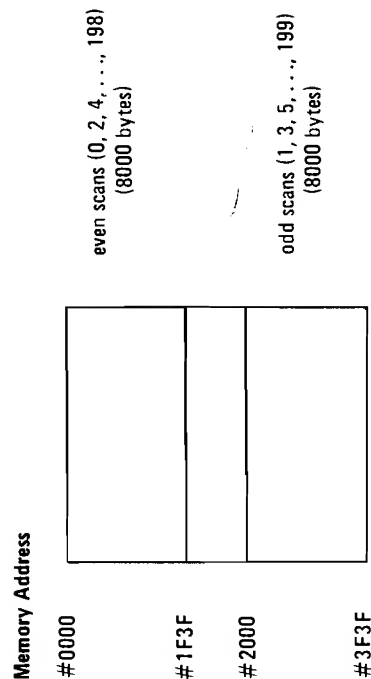
FORMAT:

7	6	5	4	3	2	1	0
C1	C0	C1	C0	C1	C0	C1	C0

First display
pel

- Graphics storage is organized in two banks of 8000 bytes each.

Graphics Storage Map



Address #0000 contains pel information for upper left corner of display area.

Color selection is determined by the following logic:
C1 and C0 will select 4 of 16 preselected colors.

This color selection (palette) is preloaded in an I/O port.

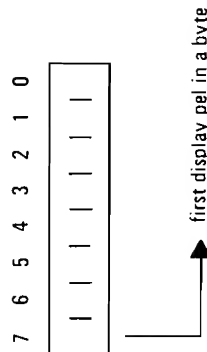
C1	C0	CODE SELECT COLOR FOR DISPLAY POSITION
0	0	DOT TAKES ON COLOR OF 1 OF 16 PRESELECTED BACKGROUND COLORS.
0	1	SELECT 1ST COLOR OF PRESELECT COLOR SET "1" OR "2"
1	0	SELECT 2ND COLOR OF PRESELECT COLOR SET "1" OR "2"
1	1	SELECT 3RD COLOR OF PRESELECT COLOR SET "1" OR "2"

The two color sets are:

SET ONE	SET TWO
COLOR 1 - CYAN	COLOR 1 - GREEN
COLOR 2 - MAGENTA	COLOR 2 - RED
COLOR 3 - WHITE	COLOR 3 - BROWN

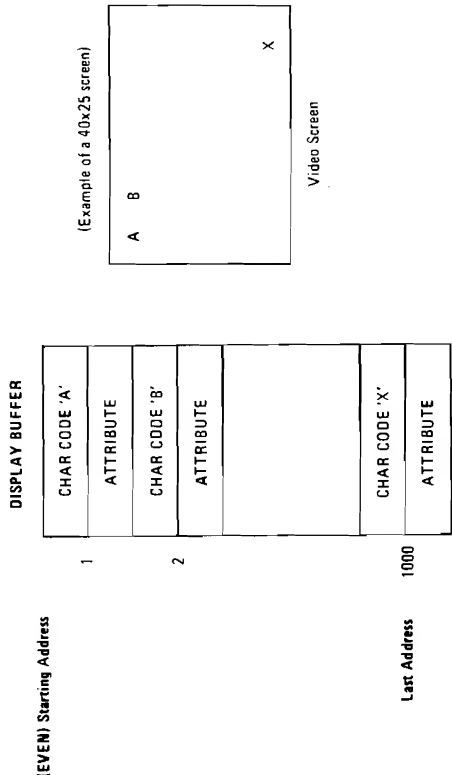
The background colors are the same basic 8 color as defined for low resolution graphic plus 8 alternate intensities defined by the intensity bit for a total of 16 color including black and white.

3. Black and white high resolution graphics (monitor)
 - Up to 200 rows of 640 pels each (1x1)
 - Black and white only
 - Requires 16000 bytes of Read/Write Memory (on the adapter)
 - Addressing and mapping is the same as for medium resolution color graphics, but the data format is different. In this mode each bit in memory is mapped to a pel on the screen.
 - 8 pels/byte



Description of Basic Operations

In the alphanumeric mode the adapter fetches character and attribute information from its display buffer. The starting address of the display buffer is programmable through the 6845, but it must be an even address. The character codes and attributes are then displayed according to their relative position in the buffer.



The CPU and the display control unit have equal access to the display buffer during all the operating modes except high resolution alphanumeric. During this mode, the CPU should access the display buffer during the vertical retrace time (if not, then the display will be affected with random patterns as the CPU is using the display buffer). The characters are displayed from a prestored "character generator" which contains the dot patterns of all the displayable characters.

In the graphics mode the displayed dots and colors are also fetched from the display buffer (up to 16K bytes). In the Color/Graphics Mode Section, the bit configuration for each graphics mode is explained.

Table 5. Summary of Available Colors

I	R	G	B	COLOR
0	0	0	0	Black
0	0	0	1	Blue
0	0	1	0	Green
0	0	1	1	Cyan
0	1	0	0	Red
0	1	0	1	Magenta
0	1	1	0	Brown
0	1	1	1	Light Gray
1	0	0	0	Dark Gray
1	0	0	1	Light Blue
1	0	1	0	Light Green
1	0	1	1	Light Cyan
1	1	0	0	Light Red
1	1	0	1	Light Magenta
1	1	1	0	Yellow
1	1	1	1	White

Note: "I" provides extra luminance (brightness) to each shade available. Resulting in the light colors listed above, except where the "I" bit is not recognized by some monitors.

Programming Considerations

Programming the 6845 CRT Controller

The 6845 has 19 internal registers which are used to define and control a raster scanned CRT display. One of these registers, the Address Register, is actually used as a pointer to the other 18 registers. It is a write only register which is loaded from the CPU by executing an OUT instruction to I/O address 3D4. The five least significant bits of the I/O bus are loaded into the Address Register.

In order to load any of the other 18 registers, the Address Register is first loaded with the necessary pointer and then the CPU may output a value to I/O address 3D5 in order to load the information in the preselected register.

The following table defines the values which must be loaded in 6845 Registers in order to control the different modes of operation supported by the attachment.

Table 6. 6845 Register Description

ADDR REG.	REG. #	REGISTER TYPE	UNITS	I/O	40x25 ALPHA	80x25 ALPHA	GRAPHIC MODES
0	R0	Horizontal Total	Char.	Write Only	38	71	38
1	R1	Horizontal Displayed	Char.	Write Only	28	50	28
2	R2	Horiz. Sync Position	Char.	Write Only	2D	5A	2D
3	R3	Horiz. Sync Width	Char.	Write Only	0A	0A	0A
4	R4	Vertical Total	Char. Row	Write Only	1F	1F	7F
5	R5	Vertical Total Adjust	Scan Line	Write Only	06	06	06
6	R6	Vertical Displayed	Char. Row	Write Only	19	19	64
7	R7	Vert. Sync Position	Char. Row	Write Only	1C	1C	70
8	R8	Interlace Mode	—	Write Only	02	02	02
9	R9	Max Scan Line Addr.	Scan Line	Write Only	07	07	01
A	R10	Cursor Start	Scan Line	Write Only	06	06	06
B	R11	Cursor End	Scan Line	Write Only	07	07	07
C	R12	Start Addr. (H)	—	Write Only	00	00	00
D	R13	Start Addr. (L)	—	Write Only	00	00	00
E	R14	Cursor Addr. (H)	—	Read/Write	XX	XX	XX
F	R15	Cursor Addr. (L)	—	Read/Write	XX	XX	XX
10	R16	Light Pen (H)	—	Read Only	XX	XX	XX
11	R17	Light Pen (L)	—	Read Only	XX	XX	XX

Note: All register values are given in hexadecimal.

Programming the Mode Control and Status Register

The following I/O devices are defined on the Color/Graphics Adapter.

HEX ADDR.	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	FUNCTION OF REGISTER
X'308'	1	1	1	1	0	1	1	0	0	0	00 REG (MODE CONTROL)
X'309'	1	1	1	1	0	1	1	0	0	1	00 REG (COLOR SELECT)
X'30A'	1	1	1	1	0	1	1	0	1	0	01 REG (STATUS)
X'30B'	1	1	1	1	0	1	1	0	1	1	CLEAR LIGHT PEN LATCH
X'30C'	1	1	1	1	0	1	1	1	0	0	PRE SET LIGHT PEN LATCH
X'30D'	1	1	1	1	0	1	0	1	0	0	6845 REGISTERS
X'30E'	1	1	1	1	0	1	0	0	1	0	6845 REGISTERS
X'30F'	1	1	1	1	0	1	0	0	1	1	6845 REGISTERS
X'310'	1	1	1	1	0	1	0	0	1	1	6845 REGISTERS

Z = don't care condition

Color Select Register

This is a 6 bit output only, register, it cannot be read, its address is X'3D9' and can be written using the 8088 I/O OUT command.

The following is a description of the Register functions.

Bit 0	B (BLUE) Border Color Select ALPHA/BACKGROUND
Bit 1	G (GREEN) Border Color Select ALPHA/BACKGROUND
Bit 2	R (RED) Border Color Select ALPHA/BACKGROUND
Bit 3	I Intensifies Border Color Select ALPHA/BACKGROUND IN 320 x 200
Bit 4	Select Alt Back Color Set For Alpha Color Modes
Bit 5	320 x 200 Color Set Select
Bit 6	Not Used
Bit 7	Not Used

Bits 0, 1, 2, 3. Select the screens border color in 40x25 alpha mode. In graphics mode (medium resolution) 320x200 color, the screen background color (C0-C1) is selected by these bit settings.

Bit 4. This bit when set will select on alternate, intensified, set of background colors in the alpha mode.

Bit 5 is only used in the medium resolution color mode (320x200). It is used to select the active set of screen colors for the display.

When bit 5 is set to a "1" colors are determined as follows:

The C1	C0	Set selected are:
0	0	Background as defined by Bit 0-3 of Port '3D9'
0	1	Cyan
1	0	Magenta
1	1	White

When bit 5 is set to a "0" colors are determined as follows:

The C0	C1	Set selected are:
0	0	Background as defined by Bit 0-3 of Port '3D9'
0	1	Green
1	0	Red
1	0	Yellow

Mode Select Register

This is a 6 bit output only register, it cannot be read. Its address is X'3D8'. It can be written using the 8088 I/O OUT command.

The following is a description of the registers functions.

Bit 0	80x25 mode
Bit 1	Graphic Select
Bit 2	B & W Select
Bit 3	Enable Video Signal
Bit 4	High Res 640x200 B & W Mode
Bit 5	Change BACKGROUND INTENSITY to Blink Bit
Bit 6	Not Used
Bit 7	Not Used

Bit 0 Selects between 40x25 and 80x25 alpha mode, a "1" sets it to 80x25 mode.

Bit 1 Selects between ALPHA mode and 320x200 graphics mode, a "1" select 320x200 graphics mode.

Bit 2 Selects color or B & W mode, a "1" selects B & W.

Bit 3 Enables the video signal at certain times when modes are being changed. The video signal should be disabled when changing modes. A "1" enables the video signal.

Bit 4 When on, this bit selects the 640x200 B & W graphics mode. One color of 8 can be selected on direct drive sets in this mode by using register 3D9.

Bit 5 When on, this bit will change the character background intensity to the blinking attribute function for ALPHA modes. When the high order attribute bit is not selected, 16 background colors (or intensified colors) are available. For normal operation, this bit should be set to "1" to allow the blinking function.

Mode Register Summary

Bits

0	1	2	3	4	5
0	0	1	1	0	1
0	0	0	1	0	1
1	0	1	1	0	1
1	0	0	1	0	1
0	1	1	1	0	z
0	1	0	1	0	z
0	1	1	1	1	z

40 x 25 ALPHA B & W

40 x 25 ALPHA COLOR

80 x 25 ALPHA B & W

80 x 25 ALPHA COLOR

320 x 200 B & W GRAPHICS

320 x 200 COLOR GRAPHICS

640 x 200 B & W GRAPHICS

ENABLE BLINK ATTRIBUTE

640 x 200 B & W

ENABLE VIDEO

SELECT B & W MODE

SELECT 320 x 200 GRAPHICS

80 x 25 ALPHA SELECT

z = don't care condition

* THE LOW RESOLUTION 160 x 100 MODE REQUIRES SPECIAL PROGRAMMING AND IS SET UP AS ALPHA MODE 40 x 25

Status Register

The status register is a 4 bit read only register. Its address is X'3DA'. It can be read using the 8088 I/O IN instruction.

The following is a description of the register functions.

- Bit 0 Display Enable
- Bit 1 Light Pen Trigger Set
- Bit 2 Light Pen SW Made
- Bit 3 Alpha Dots
- Bit 4 Not Used
- Bit 5 Not Used
- Bit 6 Not Used
- Bit 7 Not Used

Bit 0 This input bit, when active, indicates that a regen buffer memory access can be made without interfering with the Display.

Bit 1 This bit, when active, indicates that a positive going edge from the light pen input has set the light pen trigger. This trigger is reset on power on and may also be cleared by doing an I/O OUT command to address X'3DB'. No specific data setting is required, the action is address activated.

Bit 2 The light pen switch status is reflected in this status bit. The switch is not latched or debounced. A "0" indicates the switch is on.

Bit 3 The ALPHA video output signal is readable in this status bit. Its purpose is to verify that video information is being generated for RAS purposes.

Sequence of Events

1. Determine mode of operation
2. Reset Video Enable bit
3. Program 6845 to select mode
4. Program mode/color select registers

Memory Requirements

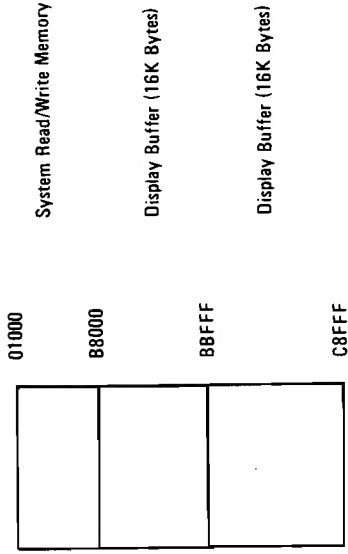
The memory used by this adapter is self-contained. It consists of 16K bytes of memory without parity. This memory is used as both a display buffer for alphanumeric data and as a bit map for graphics data. The Regen Buffers address starts at X'B8000'.

Interrupt Level (Vertical Retrace)

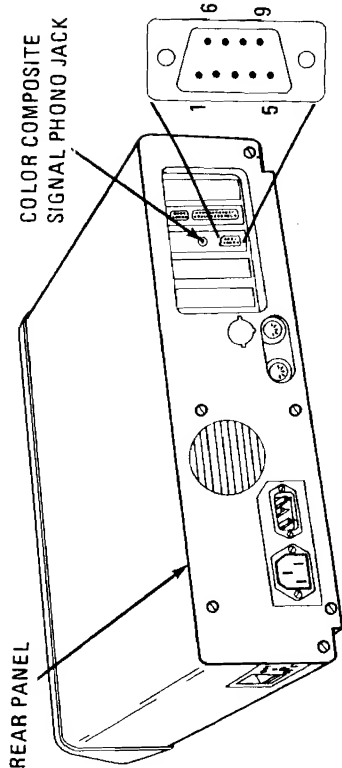
Level 2

I/O Address and Bit Map

Read/Write Memory Address Space

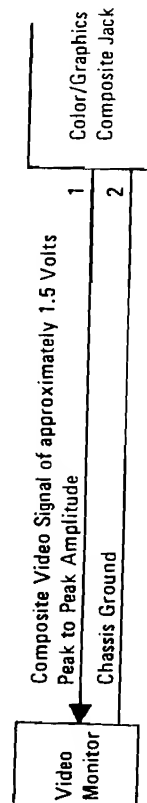
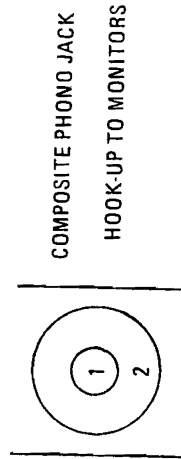
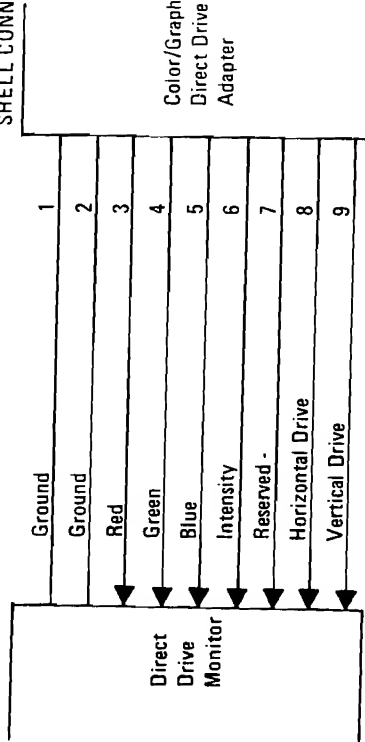


Color/Graphics Monitor Adapter Direct Drive and Composite Interface Pin Assignment

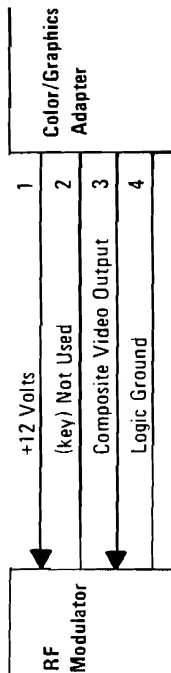
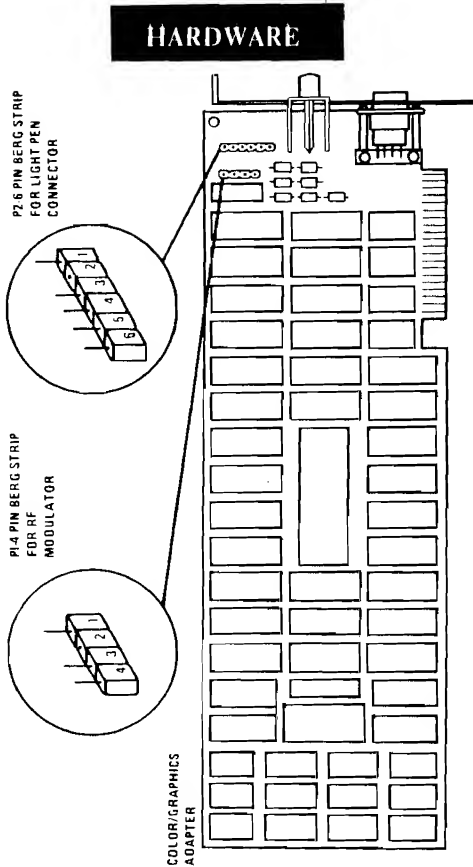


AT STANDARD TTL LEVELS

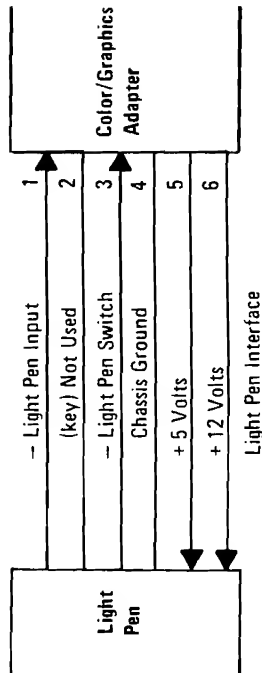
COLOR DIRECT DRIVE 9 PIN "D" SHELL CONNECTOR



Color/Graphics Monitor Adapter Auxiliary Video Connectors



RF Modulator Interface



Light Pen Interface

Parallel Printer Adapter

The Printer Adapter is specifically designed to attach printers with a parallel port interface, but it can be used as a general input/output port for any device or application which matches its input/output capabilities. It has 12 TTL buffer output points which are latched and can be written and read under program control using the processor IN or OUT instructions. The adapter also has five steady state input points that may be read using the processor's IN instructions.

In addition, one input can also be used to create a processor interrupt. This interrupt can be enabled and disabled under program control. Reset from the power-on circuit is also "ORed" with a program output point allowing a device to receive a power-on reset when the processor is reset.

This function is packaged on an adapter which fits into any of the five System Expansion slots on the System Board. The input/output signals are made available at the back of the adapter via a right angle PCB mounted 25 PIN "D" type connector. This connector protrudes through the rear panel of the System Unit where a cable and shield may be attached.

When this adapter is used to attach a printer, data, or printer, commands are loaded into an 8-bit latched output port, and the strobe line is activated writing data to the printer. The program then may read the input ports for printer status indicating when the next character can be written or it may use the interrupt line to indicate "not busy" to the software.

The output ports may also be read at the card's interface for diagnostic loop functions. This allows fault isolation determination between the adapter and the attaching device.

This same function is also part of the combination IBM Monochrome Display and Printer Adapter. A block diagram of the printer adapter is on the following page.

Parallel Printer Adapter Block Diagram

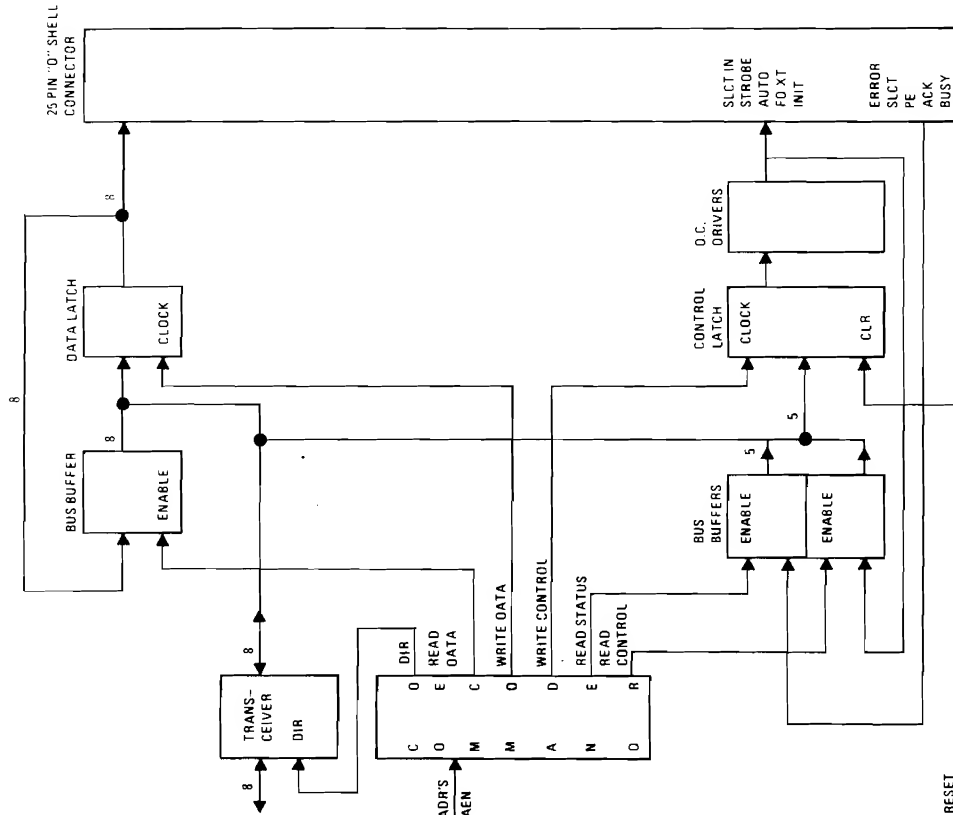


Figure 16. PARALLEL PRINTER ADAPTER BLOCK DIAGRAM

Programming Considerations

The Printer Adapter responds to 5 I/O instructions — 2 output and 3 input. The output instructions transfer data into 2 latches whose outputs are presented on pins of a 25 Pin "D" shell connector.

Two of the three input instructions allow the CPU to read back the contents of the two latches. The third allows the CPU to read the real time status of a group of pins on the connector. A description of each instruction follows.

IBM Monochrome Display & Printer Adapter				Parallel Printer Adapter			
Output to address 38CH				Output to address 378H			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2

This instruction captures data from the data bus and is present on the respective pins. These pins are each capable of sourcing 2.6 ma and sinking 24 ma.

It is essential that the external device not try to pull these lines to ground.

IBM Monochrome Display & Printer Adapter				Parallel Printer Adapter			
Output to address 38EH				Output to address 37AH			
				Bit 4	Bit 3	Bit 2	Bit 1
				IRQ Enable	Pin 17	Pin 16	Pin 14
							Pin 1

This instruction causes this latch to capture the five least significant bits of data bus. The four least significant bits present their outputs, or inverted versions of their outputs to the respective pins shown above. If bit 4 is written 1, the card will interrupt the CPU on the condition that Pin 10 transitions high to low.

These pins are driven by open collector drivers pulled to +5V through 4.7K OHM resistors. They can each sink approximately 7 ma and maintain 0.8 volts down level.

Note: For pin references, see Parallel Interface Connector Specifications, page 2-79.

IBM Monochrome Display & Printer Adapter	
Input from address x' 3BC'	Parallel Printer Adapter Input from address 378H

This command presents the CPU with data present on the pins associated with the out to x' 3BC'. This should normally reflect the exact value that was last written to x' 3BC'. If an external device should be driving data on these pins (in violation of usage ground rules) at the time of an input, this data will be 'or'ed with the latch contents.

IBM Monochrome Display & Printer Adapter	
Input from address 380H	Parallel Printer Adapter Input from address 379H

This command presents real time status to the CPU from the pins as follows.

Bit 7 Pin 11*	Bit 6 Pin 10	Bit 5 Pin 12	Bit 4 Pin 13	Bit 3 Pin 15	Bit 2 Pin 14	Bit 1 Pin 16	Bit 0 Pin 17
------------------	-----------------	-----------------	-----------------	-----------------	-----------------	-----------------	-----------------

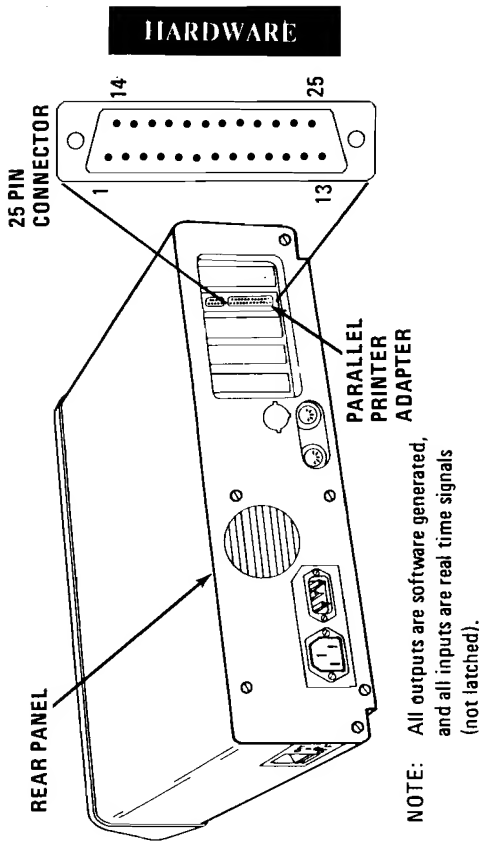
IBM Monochrome Display & Printer Adapter	
Input from address 38EH	Parallel Printer Adapter Input from address 37AH

This instruction causes the data present on pins 1, 14, 16, 17 and IRQ bit to be read by the CPU. In the absence of external drive applied to these pins, data read by the CPU will exactly match data last written to x' 3BE' in the same bit positions. Note that data bits 0-2 are not included. If external drivers are dotted to these pins, that data will be 'or'ed with data applied to the pins by the x' 3BE' latch.

Bit 7	Bit 6	Bit 5	Bit 4 IRQ Enable	Bit 3 Pin 17	Bit 2 Pin 16	Bit 1 Pin 14	Bit 0 Pin 1
			Por=0	Por=1	Por=0	Por=1	Por=1

These pins assume the states shown after a reset from the CPU.
Note: For pin references see Parallel Printer Adapter Interface Connector Specifications page 2-79.

Parallel Printer Adapter Interface Connector Specifications



AT STANDARD TTL LEVELS

Signal Name	Adapter Pin No.
- Strobe	1
+ Data Bit 0	2
+ Data Bit 1	3
+ Data Bit 2	4
+ Data Bit 3	5
+ Data Bit 4	6
+ Data Bit 5	7
+ Data Bit 6	8
+ Data Bit 7	9
- Acknowledge	10
+ Busy	11
+ P. End (out of Paper)	12
+ Select	13
- Auto Feed	14
- Error	15
- Initialize Printer	16
- Select Input	17
Ground	18 - 25

IBM 80 CPS Graphics Printer

The printer is a self powered, standalone, table top unit. It attaches to the system unit via a parallel signal cable 6 feet (1.8 meters) in length. It obtains AC power from a standard wall outlet and is available in three different versions (120, 220, or 240 Vac). The printer is an 80 Character Per Second (CPS) bidirectional wire matrix device. It prints characters in a 9x9 dot matrix with a 9 wire head. It can print in a compressed mode of 132 characters per line and in a standard font, 80 characters per line. A large font also prints in 66 characters per line mode.

The printer can print double size characters and double strike characters. It can select from two character sets, an extended upper/lower case character set for international languages, and the U.S. standard upper/lower case 96 character ASCII character set. It can print subscript, superscript, defined graphics characters, underlining, and programmable graphics.

The printer can also accept commands setting the line feed control desired for the application. It attaches to the system unit via the Parallel Printer Adapter or the IBM Monochrome Display and Printer Adapter. The cable is a 25 lead shielded cable with a 25 pin "D" type connector at the system unit end, and a 36 pin connector on the printer end.

Table 7. Printer Specifications

(1)	Print Method:	Serial Impact dot matrix												
(2)	Print Speed:	80 CPS												
(3)	Print Direction:	Bidirectional with logical seeking												
(4)	Number of Pins in Head	9												
(5)	Line Spacing:	4.23 mm (1/6 inch) or programmable												
(6)	Printing Characteristics													
	Matrix:	9x9												
	Character Set 1:	Full 96-character ASCII with descenders, additional ASCII numbers 160 to 175 are European characters. 176 to 223 are graphic characters. 224 to 239 are selected Greek characters. 240 to 255 contain math and extra symbols.												
	Character Set 2:	Same as above except: ASCII numbers 3, 4, 5, 6, and 21 contain symbols. ASCII numbers 128 to 175 contain European Characters.												
	Graphics:	20 block characters and programmable graphics.												
(7)	Printing Sizes	<table><thead><tr><th>Characters per inch</th><th>Maximum characters per line</th></tr></thead><tbody><tr><td>10</td><td>80</td></tr><tr><td>5</td><td>40</td></tr><tr><td>16.5</td><td>132</td></tr><tr><td>8.25</td><td>66</td></tr><tr><td>10</td><td>80</td></tr></tbody></table>	Characters per inch	Maximum characters per line	10	80	5	40	16.5	132	8.25	66	10	80
Characters per inch	Maximum characters per line													
10	80													
5	40													
16.5	132													
8.25	66													
10	80													
(8)	Media Handling													
	Paper Feed:	Adjustable sprocket pin feed												
	Paper Width Range:	101.6 mm (4 inches) to 254 mm (10 inches)												
	Copies:	One original plus two carbon copies, total thickness not to exceed 0.3 mm (0.012 inch). Minimum paper thickness is 0.064 mm or 0.0025 inch.												
(9)	Paper Path:	Rear												
	Interfaces Standard:	Parallel 8-bit Data Data and Control lines												
(10)	Inked Ribbon													
	Color:	Black												
	Type:	Cartridge												
	Life Expectancy:	3 million characters												

Table 7. Printer Specifications (continued)

(11)	Environmental Conditions	5 to 35°C (41 to 95° F)
		10 to 80% non-condensing
(12)	Power Requirements	Three models available:
		120 220 240
	Voltage (AC):	60 50/60 50/60
		Frequency (Hz):
	Maximum Current (Amps):	1 .5 .5
		Maximum Power (Watts):
(13)	Physical Characteristics	100 100 100
		Height:
	Width:	107 mm (4.2 inches)
	Depth:	374 mm (14.7 inches)
	Weight:	305 mm (12.0 inches)
		5.5 kg (12 lbs.)

Setting the DIP Switches

There are two DIP switches on the control circuit board. In order to suit the user's specific requirements, desired control modes are selectable by the DIP switches. The functions of the switches and their preset conditions at the time of shipment are as shown in Table 8 (DIP Switch 1) and Table 9 (DIP Switch 2).

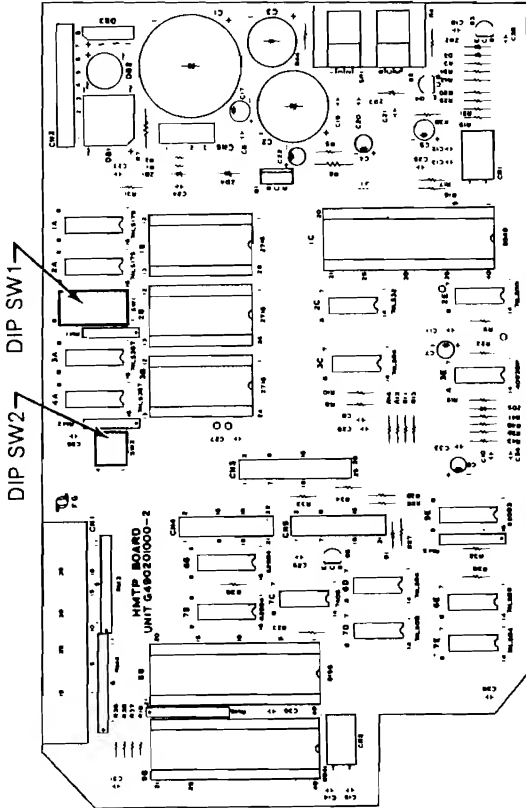


Figure 17. LOCATION OF PRINTER DIP SWITCHES

Table 8. Functions and Conditions of DIP Switch 1

Switch No.	Function	ON	OFF	Factory-set Condition
1-1	Not applicable	—	—	ON
1-2	CR	Print only	Print & line feed	ON
1-3	Buffer full	Print only	Print & line feed	OFF
1-4	Cancel code	Invalid	Valid	OFF
1-5	Not applicable	—	—	ON
1-6	Error buzzer	Sound	Does not sound	ON
1-7	Character generator	Table 2	Table 1	ON
1-8	Select in signal	Fixed internally	Not fixed internally	ON

Table 9. Functions and Conditions of DIP Switch 2

Switch No.	Function	ON	OFF	Factory-set Condition
2-1	Form length	12" 304.8 mm	11" 279.4 mm	OFF
2-2	Line spacing	1/8" 3.175 mm	1/6" 4.23 mm	OFF
2-3	Auto Feed XT signal	Fixed internally	Not fixed internally	OFF
2-4	1 inch skip over perforation	Valid	Not valid	OFF

Parallel Interface Description

- (1) Specifications
 - (a) Data transfer rate: 1000 CPS (max.)
 - (b) Synchronization: By externally supplied STROBE pulses.
 - (c) Handshaking: ACKNLG or BUSY signals.
 - (d) Logic level: Input data and all interface control signals are compatible with the TTL level.
- (2) Connector
 - Plug: 57-30360 (AMPHENOL)
- (3) Connector pin assignment and descriptions of signals.
 - Connector pin assignment and descriptions of respective interface signals are provided in Table (10) page 2-86.

Table 10. Connector Pin Assignment and Description of Interface Signals

Signal Pin No.	Return Pin No.	Signal	Direction	Description
1	19	<u>STROBE</u>	In	STROBE pulse to read data in. Pulse width must be more than 0.5 μ s at receiving terminal. The signal level is normally "HIGH"; read-in of data is performed at the "LOW" level of this signal.
2	20	DATA 1	In	These signals represent information of the 1st to 8th bits of parallel data respectively. Each signal is at "HIGH" level when data is logical "1" and "LOW" when logical "0".
3	21	DATA 2	In	
4	22	DATA 3	In	
5	23	DATA 4	In	
6	24	DATA 5	In	
7	25	DATA 6	In	
8	26	DATA 7	In	
9	27	DATA 8	In	
10	28	<u>ACKNLG</u>	Out	Approx. 5 μ s pulse. "LOW" indicates that data has been received and that the printer is ready to accept other data.
11	29	BUSY	Out	A "HIGH" signal indicates that the printer cannot receive data. The signal becomes "High" in the following cases: 1. During data entry 2. During printing operation 3. In OFF-LINE state 4. During printer error status.

Table 10. Connector Pin Assignment and Description of Interface Signals (continued)

Signal Pin No.	Return Pin No.	Signal	Direction	Description
12	30	PE	Out	A "HIGH" signal indicates that the printer is out of paper.
13	—	SLCT	Out	This signal indicates that the printer is in the selected state.
14	—	AUTO FEED XT	In	With this signal being at "LOW" level, the paper is automatically fed one line after printing. (The signal level can be fixed to "LOW" with DIP SW pin 2-3 provided on the control circuit board.)
15	—	NC		Not used.
16	—	OV		Logic GND level.
17	—	CHASSIS-GND	—	Printer chassis GND. In the printer, the chassis GND and the logic GND are isolated from each other.
18	—	NC	—	Not used.
19-30	—	GND	—	TWISTED-PAIR RETURN signal GND level.
31	—	INIT	In	When the level of this signal becomes "LOW" the printer controller is reset to its initial state and the print buffer is cleared. This signal is normally at "HIGH" level, and its pulse width must be more than 50 μ s at the receiving terminal.

Table 10. Connector Pin Assignment and Description of Interface Signals (continued)

Signal Pin No.	Return Pin No.	Signal	Direction	Description
32		ERROR	Out	The level of this signal becomes "LOW" when the printer is in— 1. PAPER END state 2. OFF-LINE state 3. Error state
33	—	GND	—	Same as with Pin No. 19 to 30.
34	—	NC	—	Not used.
35				Pulled up to +5V through 4.7K Ω resistance.
36	—	SLCT IN	In	Data entry to the printer is possible only when the level of this signal is "LOW". (Internal fixing can be carried out with DIP SW 1-8. The condition at the time of shipment is set "LOW" for this signal.)

- NOTES**
- 1: "Direction" refers to the direction of signal flow as viewed from the printer.
 - 2: "Return" denotes "TWISTED PAIR RETURN" and is to be connected at signal ground level.
As to the wiring for the interface, be sure to use a twisted-pair cable for each signal and never fail to complete connection on the Return side. To prevent noise effectively, these cables should be shielded and connected to the chassis of the System Unit and the printer, respectively.
 - 3: All interface conditions are based on TTL level. Both the rise and fall times of each signal must be less than 0.2 μ s.
 - 4: Data transfer must not be carried out by ignoring the ACKNLG or BUSY signal. (Data transfer to this printer can be carried out only after confirming the ACKNLG signal or when the level of the BUSY signal is "LOW".)

- (4) Data transfer sequence
Figure 17 shows the sequence for data transmission.

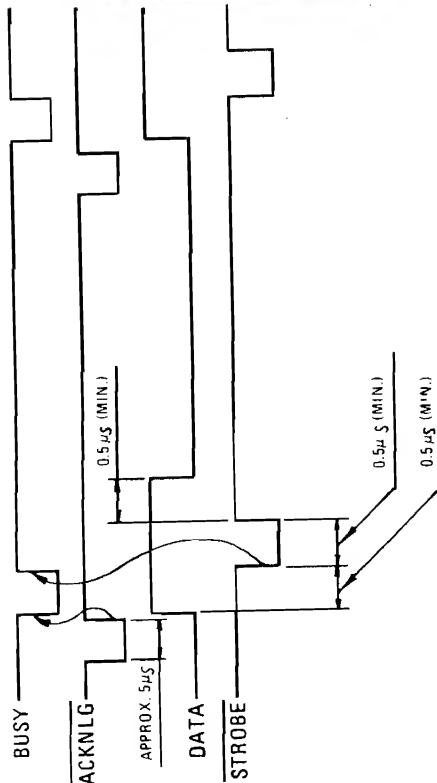


Figure 18. PARALLEL INTERFACE TIMING DIAGRAM

Below are the allowed combinations of print modes that can be selected.

The IBM 80 CPS Graphics Printer can select any of the combinations listed below and may change print modes at any place within a line.

Note: Modes can be selected and combined if they are in the same vertical column.

[illegible]

Printer Control Codes

On the following pages you will find complete codes for printer control, characters, and graphics. You may want to keep them handy for future reference. The printer codes are listed in ASCII decimal order (e.g. NUL is zero, BEL is 7, etc.). Examples given in the Printer Function descriptions are written in BASIC. The "Format" description is given when more information is needed for programming considerations. ASCII decimal values for the printer control codes can be found in the Printer Character Sets which follow these control codes.

Printer Code	Printer Function
NUL	<p>Null</p> <p>Used with ESC B and ESC D as a list terminator. NUL is also used with other Printer Control Codes to select options (e.g. ESC S).</p> <p>Example: LPRINT CHR\$(0);</p>
BEL	<p>Bell</p> <p>Sounds the printer buzzer for 1 second.</p> <p>Example: LPRINT CHR\$(7);</p>
HT	<p>Horizontal Tab</p> <p>Tabs to the horizontal tab stop. When the printer is powered on or reset, tab stops are set every eight columns. Tab stops can be changed with the ESC D command.</p> <p>Example: LPRINT CHR\$(9)</p>
LF	<p>Line Feed</p> <p>Prints data remaining in the printer buffer and spaces the paper up one line. Line spacing is 1/6 inch (4.23 mm) unless reset by ESC A, ESC 0, ESC 1, ESC 2, or ESC 3.</p> <p>Example: LPRINT CHR\$(10);</p>

Printer Code	Printer Function
VT	Vertical Tab The VT code is treated as a LF. Example: LPRINT CHR\$(11);
FF	Form Feed Advances the paper to the top of the next page. The location of the paper, when the printer is powered on or reset, determines the top of the page. The next top of page is 11 inches (279.4 mm) from that position. ESC C can be used to change the page length. Example: LPRINT CHR\$(12);
CR	Carriage Return Ends the line the printer is on and prints the data remaining in the printer buffer. (No line feed operation is initiated by the printer.) Example: LPRINT CHR\$(13);
SO	IBM Personal Computer Basic adds a Line Feed command to every Carriage Return unless you select character set 1, add 128 to the CR, and return to character set 2. (See ESC 6 and ESC 7.) Example: LPRINT "0000";CHR\$(27);CHR\$(55);CHR\$(13+128);CHR\$(27);CHR\$(54);"////"
SI	Shift Out (Double Width) Changes to the Double Width print mode. A Carriage Return, Line Feed, DC4, or CAN cancels Double Width print mode initiated with SO. See ESC W for continuous Double Width printing. Example: LPRINT CHR\$(14);
DC2	Device Control 2 (Compressed Off) Stops printing in the Compressed Character print mode. Example: LPRINT CHR\$(15);
DC4	Device Control 4 (Double Width Off) Stops printing in the Double Width print mode started by the SO command. Example: LPRINT CHR\$(20);
CAN	Cancel Clears the printer buffer without printing data. Control codes, except SO, remain in effect. Example: LPRINT CHR\$(24);
ESC	Escape Lets the printer know that the next data sent is a printer command. (See the following list of commands.) Example: LPRINT CHR\$(27);
ESC -	Escape Minus (Underline) Format: ESC -n; ESC - followed by a 1, prints all of the following data with an underline. ESC - followed by a 0 (zero), cancels the Underline print mode. Example: LPRINT CHR\$(27);CHR(45);CHR\$(1);

Printer Code	Printer Function	Printer Code	Printer Function
ESC 0	Escape Zero (1/8-inch Line Feeding) Changes paper feeding to 1/8 inch (3.175 mm). Example: LPRINT CHR\$(27);CHR\$(48);	ESC 8	Escape Eight (Ignore Paper End) Allows the printer to print to the end of the paper. The printer ignores the paper end switch. This command must be sent prior to an actual paper end. Example: LPRINT CHR\$(27);CHR\$(56);
ESC 1	Escape 1 (7/72-inch Line Feeding) Changes paper feed to 7/72 inch (2.47 mm). Example: LPRINT CHR\$(27);CHR\$(49);	ESC 9	Escape Nine (Cancel Ignore Paper End) Cancels the Ignore Paper End command. ESC 9 is selected when the printer is powered on or reset. Example: LPRINT CHR\$(27);CHR\$(57);
ESC 2	Escape Two (Starts Variable Line Feeding) ESC 2 is an execution command for ESC A. If no ESC A command has been given, line feeding returns to 1/6 inch (4.23 mm). Example: LPRINT CHR\$(27);CHR\$(50);	ESC <	Escape Less Than (Home Head) The print head will return to the left margin to print the line following ESC <. This will occur for one line only. Example: LPRINT CHR\$(27);CHR\$(60);
ESC 3	Escape Three (Variable Line Feeding) Format: ESC 3;n; (Graphics Printer only) Changes the paper feeding to n/216-inch (1/216 inch is 0.1176 mm). A value from 1 to 255 must be assigned to n. The example below sets the paper feeding to 54/216 (1/4) inch (6.35 mm). Example: LPRINT CHR\$(27);CHR\$(51);CHR\$(54);	ESC A	Escape A (Sets the variable line feeding) Format: ESC A;n; Escape A sets the line feed feeding to n/72 inch (1/72 inch is 0.3528 mm). The example below tells the printer to set line feeding to 24/72 inch (8.47 mm). ESC 2 must be sent to the printer before the line feeding will change, e.g. ESC A;24 (text) ESC 2 (text). The text following ESC A;24 will space at the previously set line-feed increments. The text following ESC 2 will be printed with new line feed increments of 24/72 inch (8.47 mm). Any increment between 1/72 and 85/72 may be used. The default for this command at power on or reset is 6/72 inch (4.23 mm). Example: LPRINT CHR\$(27);CHR\$(65);CHR\$(24);CHR\$(27);CHR\$(50);
ESC 6	Escape Six (Select Character Set 2) Selects character set 2. (See Printer Character Set 2.) Character Set 2 is selected when the printer is powered on or reset. Example: LPRINT CHR\$(27);CHR\$(54);		
ESC 7	Escape Seven (Select Character Set 1) Selects character set 1. (See Printer Character Set 1.) Example: LPRINT CHR\$(27);CHR\$(55);		

Printer Code	Printer Function
ESC C	<p>Escape C (Set lines per page)</p> <p>Format: ESC C;n;</p> <p>Sets the page length in number of lines. The ESC C command must have a value (from 1 to 127) following it to specify the number of lines desired on the page. The example below sets the page length to 55 lines. The printer defaults to 66 lines per page when powered on or reset.</p> <p>Example:</p> <pre>LPRINT CHR\$(27);CHR\$(67);CHR\$(55);</pre> <p>Escape C (Set inches per page)</p> <p>Format: ESC C;n;m;</p> <p>Sets the length of the page in inches (one inch is 25.4 mm). This command requires a value of 0 (zero) for n and a value between 1 and 22 for m.</p> <p>Example:</p> <pre>LPRINT CHR\$(27);CHR\$(67);CHR\$(0);CHR\$(12);</pre>
ESC D	<p>Escape D (Set Horizontal Tab Stops)</p> <p>Format: ESC D;n₁;n₂;...;n_k;NUL;</p> <p>Sets the horizontal tab stop positions. The example below shows the horizontal tab stop positions set at printer column positions of 10, 20 and 40. They are followed by CHR\$(0), the NUL code. They must be in ascending numerical order as shown. Tab stops can be set between 1 and 80 in normal print mode. When in the compressed print mode, tab stops can be set up to 132. Double Width characters take up two column positions. The maximum number of tabs that can be set is 28. The HT [CHR\$(9)] is used to execute a tab operation.</p> <p>Example:</p> <pre>LPRINT CHR\$(27);CHR\$(68);CHR\$(10);CHR\$(20);CHR\$(40);CHR\$(0);</pre>

Printer Code	Printer Function
ESC E	<p>Escape E (Emphasized)</p> <p>Changes the printer to the Emphasized print mode. The printer speed is reduced to half during the Emphasized print mode.</p> <p>Example:</p> <pre>LPRINT CHR\$(27);CHR\$(69);</pre>
ESC F	<p>Escape F (Emphasized Off)</p> <p>Stops printing in the Emphasized print mode.</p> <p>Example:</p> <pre>LPRINT CHR\$(27);CHR\$(70);</pre>
ESC G	<p>Escape G (Double Strike)</p> <p>Changes the printer to the Double Strike print mode. The paper is spaced 1/216 inch (0.1176 mm) before the second pass of the print head.</p> <p>Example:</p> <pre>LPRINT CHR\$(27);CHR\$(71);</pre>
ESC H	<p>Escape H (Double Strike Off)</p> <p>Stops printing in the Double Strike mode.</p> <p>Example:</p> <pre>LPRINT CHR\$(27);CHR\$(72);</pre>
ESC J	<p>Escape J (Feed Paper n/216 inch)</p> <p>Format: ESC J;n;</p> <p>When ESC J is sent to the printer, the paper will be fed n/216 of an inch. (1/216 inch is 0.1176 mm.) The value of "n" must be between 1 and 255. The example below produces a paper feed of 50/216 inch (5.88 mm). ESC J is canceled after the paper feed takes place.</p> <p>Example:</p> <pre>LPRINT CHR\$(27);CHR\$(74);CHR\$(50);</pre>

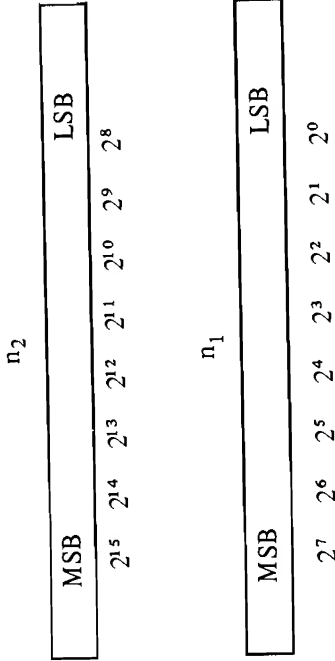
Printer Code
ESC K

Printer Function

Escape K (480 Bit Image Graphics Mode)
Format: ESC K $n_1 n_2 v_1 v_2 \dots v_k$;
Changes from the Text mode to the Bit Image Graphics mode. n_1 and n_2 are numbers, each consisting of 1 byte, which specify the total number of Bit Image Data bytes to be transferred. v_1 through v_k are the bytes of Bit Image Data whose total number (k) cannot exceed 480 and must be equal to $n_1 + 256n_2$. At every horizontal position each byte can print up to 8 vertical dots. Bit Image Data may be mixed with Text data on the same line.

Note: Assign values to n_1 and n_2 as follows: n_1 represents values from 0 - 255. n_2 represents values from 0 - 1 x 256.

MSB is Most Significant Bit and LSB is Least Significant Bit.

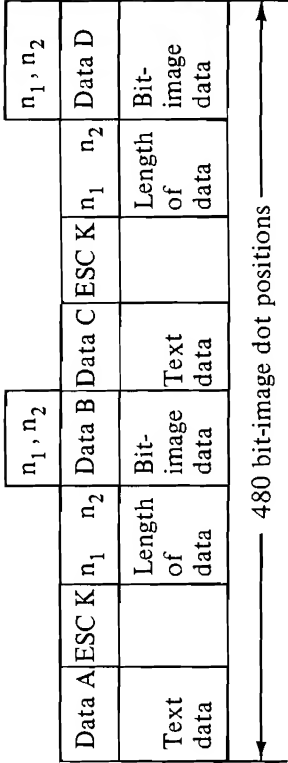


Data sent to the printer.

Text (20 characters)	ESC K n=360	Bit-image data	Next data
----------------------	-------------	----------------	-----------

20 characters in text mode correspond to 120 bit-image positions (20 x 6 = 120). The printable portion left in Bit-image mode is 360 dot positions (480 - 120 = 360).

Data sent to the printer.



HARDWARE

Example:

```

1  'OPEN PRINTER IN RANDOM MODE WITH LENGTH OF
   255
2  OPEN "LPT1:" AS #1
3  WIDTH "LPT1:",255
4  PRINT #1,CHR$(13);CHR$(10);
5  SLASH$=CHR$(1)+CHR$(2)+CHR$(4)+CHR$(8)
6  SLASH$=SLASH$+CHR$(16)+CHR$(32)+CHR$(64)
   +CHR$(128)+CHR$(0)
7  GAP$=CHR$(0)+CHR$(0)+CHR$(0)
8  NDOTS=480
9  'ESC K N1 N2
10 PRINT #1,CHR$(27);"K";CHR$(NDOTS MOD 256);
   CHR$(INT(NDOTS/256));
11 'SEND NDOTS NUMBER OF BIT IMAGE BYTES
12 FOR I=1 TO NDOTS/12 'NUMBER OF SLASHES TO
   PRINT USING GRAPHICS
13 PRINT #1,SLASH$;GAP$;
14 NEXT I
15 CLOSE
16 END
    
```

This example will give you a row of slashes printed in the 480 Bit Image mode.

Printer Code	Printer Function
ESC L	<p>Escape L (960 Bit Image Graphics Mode) Format: ESC L;n_1; n_2; v_1; v_2; ... v_k; Changes from the Text mode to the Bit Image Graphics mode. The input is similar to ESC K. The 960 Bit Image mode prints at half the speed of the 480 Bit Image mode, but can produce a denser graphic image. The number of bytes of Bit Image Data (k) is $n_1 + 256n_2$ but cannot exceed 960. n_1 is in the range of 0 to 255.</p>
ESC N	<p>Escape N (Set Skip Perforation) Format: ESC N;n; Sets the Skip Perforation function between pages. The number following ESC N sets the value for the number of lines of Skip Perforation. This value can be from 1 to 127. The example shows a 12-line skip perforation. With a page length of 66 lines this will print 54 lines and feed the paper 12 lines. ESC N is reset anytime the page length (ESC C) is changed. Example: LPRINT CHR\$(27);CHR\$(78);CHR\$(12);</p>
ESC O	<p>Escape O (Cancel Skip Perforation) Cancels the Skip Perforation function. Example: LPRINT CHR\$(27);CHR\$(79);</p>
ESC S	<p>Escape S (Subscript/Superscript) Format: ESC S;n; Changes the printer to the Subscript print mode when ESC S is followed by a 1 as in the example below. When ESC S is followed by a 0 (zero), the printer will print in the Superscript print mode. Example: LPRINT CHR\$(27);CHR\$(83);CHR\$(1);</p>
ESC T	<p>Escape T (Subscript/Superscript Off) The printer stops printing in the Subscript or Superscript print mode. Example: LPRINT CHR\$(27);CHR\$(84);</p>
ESC U	<p>Escape U (Unidirectional Printing) Format: ESC U;n; The printer will print only from left to right following the input of ESC U;1. When ESC U is followed by a 0 (zero), the left to right printing operation is canceled. The Unidirectional print mode (ESC U) assures a more accurate printing start position for better print quality. Example: LPRINT CHR\$(27);CHR\$(85);CHR\$(1);</p>
ESC W	<p>Escape W (Double Width) Format: ESC W;n; Changes to the Double Width mode when ESC W is followed by a 1. This mode is not canceled by a line feed operation or by the DC4 code. It must be canceled with ESC W followed by a 0 (zero). Example: LPRINT CHR\$(27);CHR\$(87);CHR\$(1);</p>
ESC Y	<p>Escape Y (960 Bit Image Graphics Mode) Format: ESC Y n_1; n_2; v_1; v_2; ... v_k; Changes from the Text mode to the 960 Bit Image Graphics mode. The printer prints at normal speed during this operation and cannot print dots on consecutive dot positions. The input of data is similar to ESC L.</p>
ESC Z	<p>Escape Z (1920 Bit Image Graphics Mode) Format: ESC Z;n_1; n_2; v_1; v_2; ... v_k; Changes from the Text mode to the 1920 Bit Image Graphics mode. The input is similar to the other Bit Image Graphics modes during this operation. ESC Z prints at normal speed but can only print every third dot position.</p>

Table 11. Graphics Printer Character Set 1

0	1	2	3	4	5	6	7	8	9
NUL							BEL		HT
10	11	12	13	14	15	16	17	18	19
LF	VT	FF	CR	SO	SI			DC2	
20	21	22	23	24	25	26	27	28	29
DC4				CAN			ESC		
30	31	32	33	34	35	36	37	38	39
		SP	!	"	#	\$	%	&	'
40	41	42	43	44	45	46	47	48	49
()	*	+	,	-	.	/	0	1
50	51	52	53	54	55	56	57	58	59
2	3	4	5	6	7	8	9	:	;
60	61	62	63	64	65	66	67	68	69
<	=	>	?	@	A	B	C	D	E
70	71	72	73	74	75	76	77	78	79
F	G	H	I	J	K	L	M	N	O
80	81	82	83	84	85	86	87	88	89
P	Q	R	S	T	U	V	W	X	Y
90	91	92	93	94	95	96	97	98	99
Z	[\]	^	_	`	a	b	c
100	101	102	103	104	105	106	107	108	109
d	e	f	g	h	i	j	k	l	m
110	111	112	113	114	115	116	117	118	119
n	o	p	q	r	s	t	u	v	w
120	121	122	123	124	125	126	127	128	129
x	y	z	{		}	~		NUL	

Table 11. Graphics Printer Character Set 1 (continued)

130	131	132	133	134	135	136	137	138	139
					BEL		HT	LF	VT
140	141	142	143	144	145	146	147	148	149
FF	CR	SO	SI		DC2		DC4		
150	151	152	153	154	155	156	157	158	159
		CAN			ESC				
160	161	162	163	164	165	166	167	168	169
á	í	ó	ú	ñ	Ñ	ä	ö	¿	┐
170	171	172	173	174	175	176	177	178	179
┐	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256	1/512
180	181	182	183	184	185	186	187	188	189
┐	┐	┐	┐	┐	┐	┐	┐	┐	┐
190	191	192	193	194	195	196	197	198	199
┐	┐	┐	┐	┐	┐	┐	┐	┐	┐
200	201	202	203	204	205	206	207	208	209
┐	┐	┐	┐	┐	┐	┐	┐	┐	┐
210	211	212	213	214	215	216	217	218	219
┐	┐	┐	┐	┐	┐	┐	┐	┐	┐
220	221	222	223	224	225	226	227	228	229
┐	┐	┐	┐	┐	┐	┐	┐	┐	┐
230	231	232	233	234	235	236	237	238	239
μ	τ	ϑ	Θ	Ω	δ	∞	∅	ε	∩
240	241	242	243	244	245	246	247	248	249
≡	±	≈	≠	∫	∫	÷	≈	°	■
250	251	252	253	254	255				
-	√	∩	2	■	SP				

Table 12. Graphics Printer Character Set 2

0	1	2	3	4	5	6	7	8	9
NUL			♥	♦	♣	♠	BEL		HT
10	11	12	13	14	15	16	17	18	19
LF	VT	FF	CR	SO	SI			DC2	
20	21	22	23	24	25	26	27	28	29
DC4	§			CAN			ESC		
30	31	32	33	34	35	36	37	38	39
		SP	!	"	#	\$	%	&	'
40	41	42	43	44	45	46	47	48	49
()	*	+	,	-	.	/	0	1
50	51	52	53	54	55	56	57	58	59
2	3	4	5	6	7	8	9	:	;
60	61	62	63	64	65	66	67	68	69
<	=	>	?	@	A	B	C	D	E
70	71	72	73	74	75	76	77	78	79
F	G	H	I	J	K	L	M	N	O
80	81	82	83	84	85	86	87	88	89
P	Q	R	S	T	U	V	W	X	Y
90	91	92	93	94	95	96	97	98	99
Z	[\]	^	_	`	a	b	c
100	101	102	103	104	105	106	107	108	109
d	e	f	g	h	i	j	k	l	m
110	111	112	113	114	115	116	117	118	119
n	o	p	q	r	s	t	u	v	w
120	121	122	123	124	125	126	127	128	129
x	y	z	{		}	~		Ç	ü

Table 12. Graphics Printer Character Set 2 (continued)

130	131	132	133	134	135	136	137	138	139
é	â	ä	à	â	ç	ê	ë	è	ï
140	141	142	143	144	145	146	147	148	149
î	ï	Ä	Ä	É	æ	Æ	ô	ö	ò
150	151	152	153	154	155	156	157	158	159
û	ù	ÿ	ö	ü	ç	£	¥	₣	₣
160	161	162	163	164	165	166	167	168	169
á	í	ó	ú	ñ	ã	ü	¿		
170	171	172	173	174	175	176	177	178	179
½	¼	¾	¾	¾	¾	¾	¾	¾	¾
180	181	182	183	184	185	186	187	188	189
¡	¡	¡	¡	¡	¡	¡	¡	¡	¡
190	191	192	193	194	195	196	197	198	199
¡	¡	¡	¡	¡	¡	¡	¡	¡	¡
200	201	202	203	204	205	206	207	208	209
¡	¡	¡	¡	¡	¡	¡	¡	¡	¡
210	211	212	213	214	215	216	217	218	219
¡	¡	¡	¡	¡	¡	¡	¡	¡	¡
220	221	222	223	224	225	226	227	228	229
■	■	■	■	■	■	■	■	■	■
230	231	232	233	234	235	236	237	238	239
μ	τ	θ	Ω	δ	∞	∅	ε	∩	
240	241	242	243	244	245	246	247	248	249
≡	±	≥	≤	∫	∫	÷	≈	°	■
250	251	252	253	254	255				
-	√	∩	2	■	SP				

5 1/4-Inch Diskette Drive Adapter

The System Unit has space and power for one or two 5-1/4" Diskette Drives. The drives are soft sectored, single or double sided, with 40 tracks per side. They are Modified Frequency Modulation (MFM) coded in 512 byte sectors, giving a formatted capacity of 163,840 bytes per drive for single sided and 327,680 bytes per drive for double sided. They have a track to track access time of 8 ms and a motor start time of 500 ms.

The 5-1/4" Diskette Drive Adapter fits in one of the System Board's five System Expansion Slots. It attaches to the two drives via an internal daisy chained flat cable which connects to one end of the drive adapter. The adapter has a second connector on the other end which extends through the rear panel of the System Unit. This connector contains the signals for two additional external drives, thus the 5-1/4" Diskette Drive Adapter is capable of attaching four 5-1/4" drives, two internal, and two external.

The adapter is designed for double density MFM coded drives and uses write precompensation with an analog phase locked loop for clock and data recovery. The adapter is a general purpose device using the NEC μ PD765 compatible controller. Thus the drive parameters are programmable. In addition, the attachment supports the drive's write protect feature.

The adapter is buffered on the I/O bus and uses the System Board direct memory access (DMA) for record data transfers. An interrupt level is also used to indicate operation complete and status condition requiring processor attention.

In general, the 5-1/4" Diskette Drive Adapter presents a high-level command interface to software I/O drivers. A block diagram of the 5-1/4" Diskette Drive Adapter is on the following page.

5-1/4" Diskette Drive Adapter Block Diagram

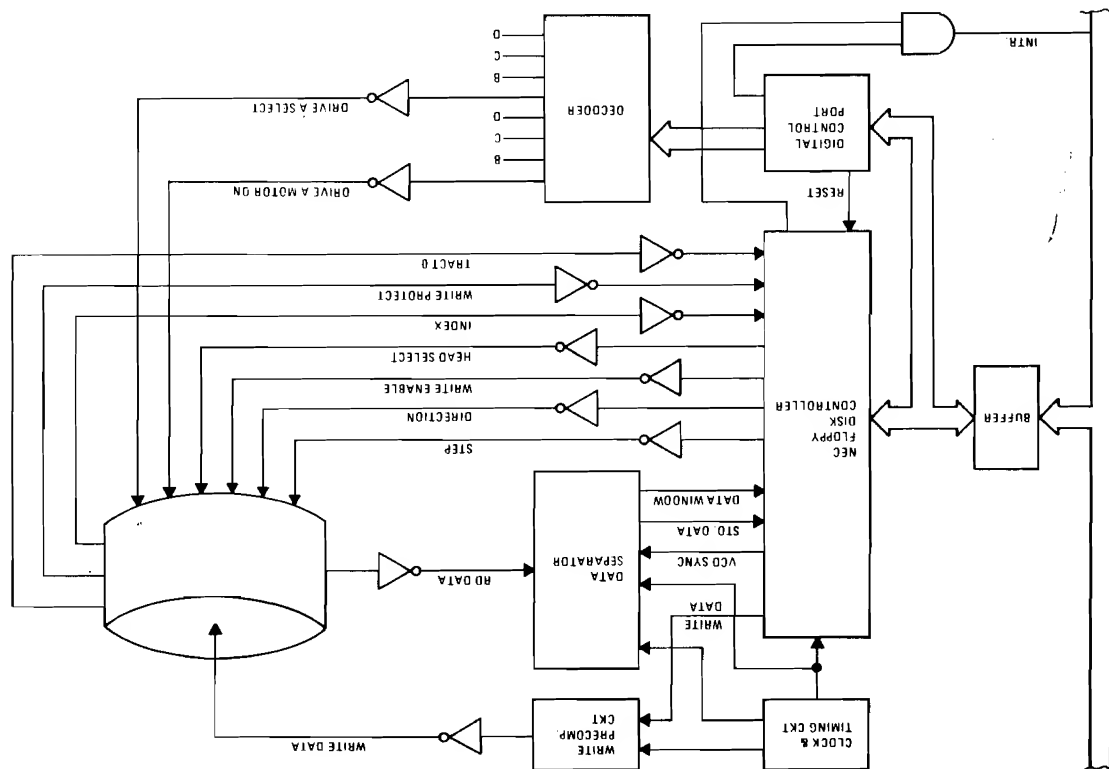


Figure 19. 5 1/4" DISKETTE DRIVE ADAPTER BLOCK DIAGRAM

Functional Description

From a programming point of view, this attachment consists of an 8-bit digital output register in parallel with a NEC μ PD765 or equivalent Floppy Disk Controller (FDC).

In the following description, drives numbers 0-3 are equivalent to drives A-D respectively.

Digital Output Register (DOR)

The Digital Output Register (DOR) is an output only register used to control drive motors, drive selection, and feature enable. All bits are cleared by the I/O interface reset line. The bits have the following functions:

Bits 0 and 1 These bits are decoded by the hardware to select one drive if its motor is on:

Bit	1	0	Drive
0	0	0	A
0	1	1	B
1	0	2	C
1	1	3	D

Bit 2 The FDC is held reset when this bit is clear. It must be set by the program to enable the FDC.

Bit 3 This bit allows the FDC interrupt and DMA requests to be gated onto the I/O interface. If this bit is cleared, the interrupt and DMA request I/O interface drivers are disabled.

Bits 4,5,6, and 7 These bits control respectively the motors of drives 0,1,2,A,B,C, and 3,D. If a bit is clear, the associated motor is off, and the drive cannot be selected.

Floppy Disk Controller (FDC)

The following is a brief summary of the registers and commands implemented by the FDC.

The FDC contains two registers which may be accessed by the main system processor; a Status Register and a Data Register. The 8-bit Main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (actually consisting of several registers in a stack with only one register presented to the data bus at a time) stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to

program or obtain the results after a particular command. The Main Status Register may only be read and is used to facilitate the transfer of data between the processor and FDC.

The bits in the Main Status Register are defined as follows:

Bit Number	Name	Symbol	Description
DB0 FDD	FDD A Busy	DAB	FDD number is in the Seek mode.
DB1	FDD B Busy	DBB	FDD number 1 is in the Seek mode.
DB2	FDD C Busy	DCB	FDD number 2 is in the Seek mode.
DB3	FDD D Busy	DDB	FDD number 3 is in the Seek mode.
DB4	FDC Busy	CB	A read or write command is in process.
DB5	Non-DMA Mode	NDM	The FDC is in the non-DMA mode.
DB6	Data Input/	DIO	Indicates direction of data transfer between FDC and Processor. If DIO = "1", then transfer is from FDC Data Register to the Processor. If DIO = "0", then transfer is from the Processor to FDC Data Register.
DB7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM should be used to perform the handshaking functions of "ready" and "direction" to the processor.

The FDC is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the FDC and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase

The FDC receives all information required to perform a particular operation from the processor.

Execution Phase

The FDC performs the operation it was instructed to do.

Result Phase

After completion of the operation, status and other housekeeping information are made available to the processor.

Programming Considerations

Table 13. Symbol Description

The following tables define the symbols used in the command summary which follows.

SYMBOL	NAME	DESCRIPTION
A0	Address Line 0	A0 controls selection of Main Status Register (A0 = 0) or Data Register (A0 = 1).
C	Cylinder Number	C stands for the current/selected Cylinder (track) number of the medium.
D	Data	D stands for the data pattern which is going to be written into a Sector.
D7-D0	Data Bus	8-bit Data Bus, where D7 stands for a most significant bit, and D0 stands for a least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector.
EOT	End of Track	EOT stands for the final Sector number on a Cylinder.
GPL	Gap Length	GPL stands for the length of Gap 3 (spacing between Sectors excluding VCO Sync. Field).
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1. (H = HD in all command words.)
HLT	Head Load Time	HLT stands for the head load time in the FDD (4 to 512 ms in 4 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (0 to 480 ms in 32 ms increments.)
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected only if MFM is implemented.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. (A cylinder under both HD0 and HD1 will be read or written.)
N	Number	N stands for the number of data bytes written in a Sector.
NCN	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head.

Table 13. Symbol Descriptions (continued)

SYMBOL	NAME	DESCRIPTION
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for Cylinder number at the completion of SENSE INTERRUPT STATUS Command, indicating the position of the Head at present time.
R	Record	R stands for the Sector number, which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD. (2 to 32 ms in 2 ms increments.)
ST 0 ST 1 ST 2 ST 3	Status 0 Status 1 Status 2 Status 3	ST 0-3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A0 = 0). ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command.
STP	Scan Test	During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA), and if STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	US stands for a selected drive number encoded the same as bits 0 and 1 of the digital register (DOR) p 2-91

Command Summary

0 indicates 'logical 0' for that bit, 1 means 'logical 1', X means 'don't care'.

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	Sector ID information prior to Command execution
	W				C					
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										
Result	R				ST 0					Data-transfer between the FDD and main-system Status information after Command execution
	R				ST 1					
	R				ST 2					
	R				C					Sector ID information after Command execution
	R				H					
	R				R					
	R				N					
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	Sector ID information prior to Command execution
	W				C					
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										
Result	R				ST 0					Data-transfer between the FDD and main-system Status information after command execution
	R				ST 1					
	R				ST 2					
	R				C					Sector ID information after command execution
	R				H					
	R				R					
	R				N					
Command	W	MT	MF	SK	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	Sector ID information to command execution
	W				C					
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										
Result	R				ST 0					Data-transfer between the main-system and FDD Status information after command execution
	R				ST 1					
	R				ST 2					
	R				C					Sector ID information after command execution
	R				H					
	R				R					
	R				N					

Command Summary (continued)

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	Sector ID information prior to command execution
	W				C					
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										
Result	R				ST 0					Data-transfer between FDD and main-system Status ID information after command execution
	R				ST 1					
	R				ST 2					
	R				C					
	R				H					
	R				R					
	R				N					
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	Sector ID information prior to command execution
	W				C					
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										
Result	R				ST 0					Data-transfer between the FDD and main-system. FDC reads all of cylinders contents from index hole to EOT.
	R				ST 1					Status information after command execution
	R				ST 2					
	R				C					
	R				H					
	R				R					Sector ID information after command execution
	R				N					
Command	W	0	MF	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	The first correct ID information on the cylinder is stored in data register.
	W									Status information after command execution
	W									
	W									
	W									
	W									
	W									
Execution										
Result	R				ST 0					Sector ID information during execution phase
	R				ST 1					
	R				ST 2					
	R				C					
	R				H					
	R				R					
	R				N					

Command Summary (continued)

PHASE	R/W	DATA BUS										REMARKS
Command	W	D7	D6	D5	D4	D3	D2	D1	D0			Command Codes
Execution	W	0	MF	0	0	1	1	0	0			Bytes/Sector
Result	W	X	X	X	X	X	HD	US1	US0			Sector/Track
	W				N							Gap 3
	W				SC							filler byte
	W				GPL							FDC formats an entire
	W				D							cylinder
	R				ST 0							Status information
	R				ST 1							after command
	R				ST 2							execution
	R				C							In this case, the ID
	R				H							information has no
	R				H							meaning
	R				N							
Command	W	MT	MF	SK	1	0	0	0	1			Command Codes
Execution	W	X	X	X	X	X	HD	US1	US0			Sector ID information
Result	W				C							prior to command
	W				H							execution
	W				R							Data compared between
	W				N							the FDD and main-system
	W				EDT							Status information after
	W				GPL							command execution
	W				STP							Sector ID information
	W				ST 0							
	R				ST 1							
	R				ST 2							
	R				C							
	R				H							
	R				R							
	R				N							
Command	W	MT	MF	SK	1	1	0	0	1			Command Codes
Execution	W	X	X	X	X	X	HD	US1	US0			Sector ID information
Result	W				C							prior to command
	W				H							execution
	W				R							Data compared between
	W				N							the FDD and main-system
	W				EDT							Status information after
	W				GPL							command execution
	W				STP							Sector ID information
	W				ST 0							
	R				ST 1							
	R				ST 2							
	R				C							
	R				H							
	R				R							
	R				N							

Command Summary (continued)

PHASE	R/W	DATA BUS										REMARKS
Command	W	D7	D6	D5	D4	D3	D2	D1	D0			Command Codes
Execution	W	MT	MF	SK	1	1	1	0	1			Sector ID information
Result	W	X	X	X	X	X	HD	US1	US0			prior to command
	W				C							execution
	W				H							Data compared between
	W				R							the FDD and main-system
	W				N							Status information after
	W				EDT							command execution
	W				GPL							
	W				STP							Sector ID information
	R				ST 0							
	R				ST 1							
	R				ST 2							
	R				C							
	R				H							
	R				R							
	R				N							
Command	W	0	0	0	0	0	1	0	0			Command Codes
Execution	W	X	X	X	X	X	0	1	1			Head retracted to track 0
No Result	W											
Phase												
Command	W	0	0	0	0	1	0	0	0			Command Codes
Result	R											Status information at
	R											the end of seek opera-
	R											tion about the FDC
Command	W	0	0	0	0	0	0	1	1			Command Codes
No Result	W											
Phase	W											
Command	W	0	0	0	0	0	1	0	0			Command Codes
Result	W	X	X	X	X	X	HD	US1	US0			Status information
	R											about FDD
Command	W	0	0	0	0	1	1	1	1			Command Codes
Execution	W	X	X	X	X	X	HD	US1	US0			Head is positioned
No Result	W											over proper cylinder
Phase	W											on diskette
Command	W	0	0	0	0	1	1	1	1			Command Codes
Result	R											Invalid command codes
												(NoOp - FDC goes into
												standby state)
												ST 0 = 80

Table 14. Status Register 0

NO.	BIT		DESCRIPTION
	NAME	SYMBOL	
D7	Interrupt Code	IC	D7 = 0 and D6 = 0 Normal termination of command, (NT), Command was completed and properly executed. D7 = 0 and D6 = 1 Abnormal termination of command, (AT). Execution of command was started, but was not successfully completed. D7 = 1 and D6 = 0 Invalid command issue (IC). Command which was issued was never started. D7 = 1 and D6 = 1 Abnormal termination because during command execution the ready signal from FDD changed state.
D5	Seek End	SE	When the FDC completes the Seek command, this flag is set to 1 (high).
D4	Equipment Check	EC	If a fault signal is received from the FDD, or if the track 0 signal fails to occur after 77 step pulses (recalibrate command) then this flag is set.
D3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to side 1 of a single sided drive, then this flag is set.
D2	Head Address	HD	This flag is used to indicate the state of the head at interrupt.
D1 D0	Unit Select 1 Unit Select 0	US 1 US 0	These flags are used to indicate a Drive unit Number at interrupt.

Table 15. Status Register 1

NO.	BIT		DESCRIPTION
	NAME	SYMBOL	
D7	End of Cylinder	EN	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.
D6	—	—	Not used. This bit is always 0 (low).
D5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D4	Over Run	OR	If the FDC is not serviced by the main-systems during data transfers within a certain time interval, this flag is set.
D3	—	—	Not used. This bit is always 0 (low).
D2	No Data	ND	During Execution of a Read Data, Write Deleted Data, or Scan command, if the FDC cannot find the sector specified in the ID register, this flag is set. During execution of the Read ID command, if the FDC cannot read the ID field without an error, then this flag is set. During the execution of the Read-a-Cylinder command, if the starting sector cannot be found, then this flag is set.
D1	Not Writable	NW	During Execution of a Write Data, Write Deleted Data, or Format a Cylinder command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.

Table 16. Status Register 2

NO.	BIT		DESCRIPTION
	NAME	SYMBOL	
D7	—	—	Not Used. This bit is always 0 (low).
D6	Control Mark	CM	During execution of the Read Data or Scan command, if the FDC encounters a sector which contains a Deleted Data Address Mark, this flag is set.
D5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data then this flag is set.
D4	Wrong Cylinder	WC	This bit is related with the ND bit, and when the contents of C on the medium are different from that stored in the ID Register, this flag is set.
D3	Scan Equal Hit	SH	During execution of the Scan command, if the condition of "equal" is satisfied, this flag is set.
D2	Scan Not Satisfied	SN	During execution of the Scan command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set.
D1	Bad Cylinder	BC	This bit is related with the ND bit, and when the contents of C on the medium are different from that stored in the ID Register, and the content of C is FF, then this flag is set.
D0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.

Table 17. Status Register 3

NO.	BIT		DESCRIPTION
	NAME	SYMBOL	
D7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D5	Ready	RY	This bit is used to indicate the status of the Ready signal from the FDD.
D4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D2	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D1	Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D0	Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

Programming Summary

DPC Registers (Ports)

FDC Data Reg

I/O Address 3F5

FDC Main Status Reg

I/O Address 3F4

Digital Output Reg

I/O Address 3F2

Bit 0 Drive

00: DR #A 10: DR #C

1 Select

01: DR #B 11: DR #D

2 Not FDC Reset

3 Enable INT & DMA Requests

4 Drive A Motor Enable

5 Drive B Motor Enable

6 Drive C Motor Enable

7 Drive D Motor Enable

All bits cleared with channel reset.

Interrupt 6**DMA 2****100 Disk Format**

1 Head, 45 cylinders, 8 sectors/TRK, 512 bytes/sector, MFM.

FDC Constants

N: H'02', SC: 08, HUT: F, SRT: C, GPL FORMAT: H'05',
GPL RD/WR: 2A, HLT: 01, (8ms track-track)

Drive Constants

HD Load 35 ms
HD Settle 25 ms
Motor Start 500 ms

Comments

1. Head loads with drive select, wait HD Load time before RD/WR.
2. Following access, wait HD Settle time before RD/WR.
3. Drive motors should be off when not in use. Only A or B and C or D may run simultaneously. Wait Motor Start time before RD/WR.
4. Motor must be on for drive to be selected.
5. Data Errors can occur while using a Home Television as the system display. Locating the TV too close to the diskette area can cause this to occur. To correct the problem, move the TV away from, or to the opposite side of the System Unit.

System I/O Channel Interface

All signals are TTL compatible:

MPUL 5.5 Vdc
LPUL 2.7 Vdc
MPDL 0.5 Vdc
LPDL -0.5 Vdc

The following lines are used by this adapter.

+D0-7 (Bidirectional, Load: 1 74LS; Driver: 74LS 3-state)

These eight lines form a bus by which all commands, status, and data are transferred. Bit 0 is the low-order bit.

+A0-9

(Adapter Input, Load: 1 74LS)

These ten lines form an address bus by which a register is selected to receive or supply the byte transferred via lines D0-7. Bit 0 is the low-order bit.

+AEN

(Adapter Input, Load: 1 74LS)

The content of lines A0-9 is ignored if this line is active.

-IOW

(Adapter Input, Load: 1 74LS)

The content of lines D0-7 is stored in the register addressed by lines A0-9 or DACK2 at the trailing edge of this signal.

-IOR

(Adapter Input, Load: 1 74LS)

The content of the register addressed by lines A 0-9 or DACK2 is gated onto lines D0-7 when this line is active.

-DACK2

(Adapter Input, Load: 2 74LS)

This line active negates output DRQ2, selects the FDC data register as the source/destination of bus D0-7, and indirectly gates T/C to IRQ6.

+T/C

(Adapter Input, Load: 4 74LS)

This line and DACK2 active indicates that the byte of data for which the DMA count was initialized is now being transferred.

+RESET

(Adapter Input, Load: 1 74LS)

An up level aborts any operation in process and clears the Digital Output Register (DOR).

+DRQ2

(Adapter Output, Driver: 74LS 3-state)

This line is made active when the attachment is ready to transfer a byte of data to or from main storage. The line is made inactive by DACK2 becoming active or an I/O read of the FDC data register.

+IRQ6

(Adapter Output, Driver: 74LS 3-state)

This line is made active when the FDC has completed an operation. It results in an interrupt to a routine which should examine the FDC result bytes to reset the line and determine the ending condition.

Drive A & B Interface

All signals are TTL compatible:

MPUL 5.5 Vdc
LPUL 2.4 Vdc
MPDL 0.4 Vdc
LPDL -0.5 Vdc

All adapter outputs are driven by open-collector gates. The drive(s) must provide termination networks to Vcc (except Motor Enable 1 which has a 2K ohm resistor to Vcc).

Each adapter input is terminated with a 150 ohm resistor to Vcc.

Adapter Outputs

-Drive Select A&B

(Driver: 7438)

These two lines are used by drives A&B to degate all drivers to the adapter and receivers from the attachment (except Motor Enable) when the line associated with a drive is inactive.

-Motor Enable A&B

(Driver: 7438)

The drive associated with each of these lines must control its spindle motor such that it starts when the line becomes active and stops when the line becomes inactive.

-Step

(Driver: 7438)

The selected drive moves the read/write head one cylinder in or out per the direction line for each pulse present on this line.

-Direction

(Driver: 7438)

For each recognized pulse of the step line the read/write head moves one cylinder toward the spindle if this line is active, and away from the spindle if inactive.

-Head Select

(Driver: 7438)

Head 1 (upper head) will be selected when this line is active (low).

-Write Data

(Driver: 7438)

For each inactive to active transition of this line while Write Enable is active, the selected drive causes a flux change to be stored on the disk.

Adapter Inputs

-Write Enable

(Driver: 7438)

The drive disables write current in the head unless this line is active.

-Index

The selected drive supplies one pulse per disk revolution on this line.

-Write Protect

The selected drive makes this line active if a write protected diskette is mounted in the drive.

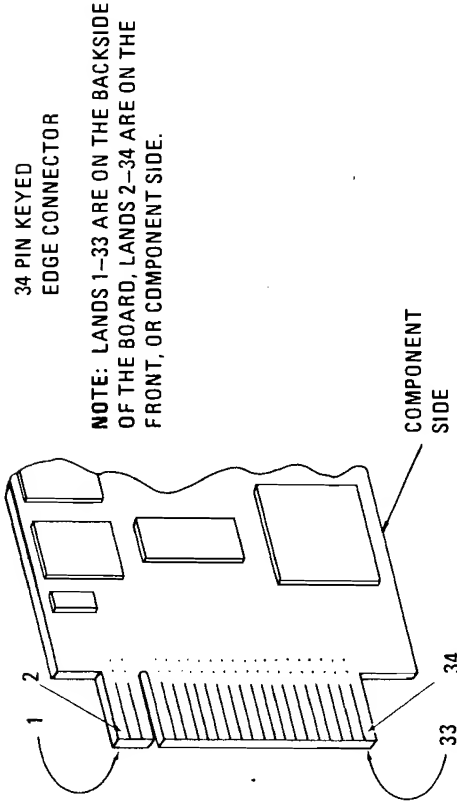
-Track 0

The selected drive makes this line active if the read/write head is over track 0.

-Read Data

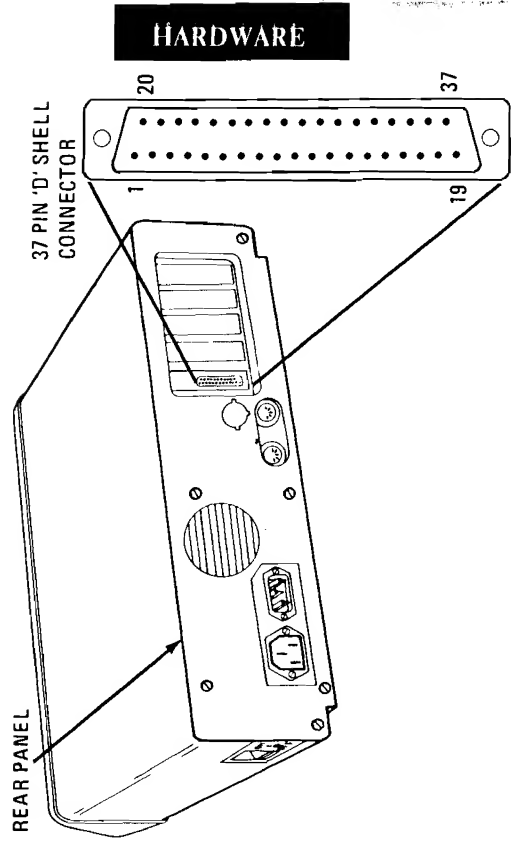
The selected drive supplies a pulse on this line for each flux change encountered on the disk.

5-1/4" Diskette Drive Adapter Internal Interface Specifications



AT STANDARD TTL LEVELS		Land No.
IBM 5 1/4" Diskette Drives	Ground-Odd Numbers	1-33
	Unused	2,4,6
	Index	8
	Motor Enable A	10
	Drive Select B	12
	Drive Select A	14
	Motor Enable B	16
	Direction (Stepper Motor)	18
	Step Pulse	20
	Write Data	22
	Write Enable	24
	Track 0	26
	Write Protect	28
	Read Data	30
	Select Head 1	32
	Unused	34
5 1/4" Diskette Drive Adapter		

5-1/4" Diskette Drive Adapter External Interface Specifications



HARDWARE

AT STANDARD TTL LEVELS		Pin no.
External Drives	Unused	1-5
	Index	6
	Motor Enable C	7
	Drive Select D	8
	Drive Select C	9
	Motor Enable D	10
	Direction (Stepper Motor)	11
	Step Pulse	12
	Select Head 1	13
	Write Enable	14
	Track 0	15
	Write Protect	16
	Read Data	17
	Write Data	18
	Ground	20-37
5 1/4" Diskette Drive Adapter		

5-1/4" Diskette Drive

The IBM 5-1/4" Diskette Drive is a single or double sided, double density, 40 track per side unit. The Diskette Drive has a formatted capacity of 163,840 bytes for single sided and 327,680 bytes for double sided, and is capable of reading and recording digital data using Modified Frequency Modulation (MFM) methods. User access for diskette loading is provided by way of a slot located at the front of the unit.

The Diskette Drive is fully self-contained and requires no operator intervention during normal operation. The Drive consists of a spindle drive system, a head positioning system, and read/write/erase system.

When the front latch is opened, access is provided for the insertion of a diskette. The diskette is positioned in place by plastic guides, and the front latch. In/out location is ensured when the diskette is inserted until a back stop is encountered.

Closing the front latch activates the cone/clamp system resulting in centering of the diskette and clamping of the diskette to the drive hub. The drive hub is driven at a constant speed of 300 rpm by a servo controlled DC motor. In operation, the magnetic head is loaded into contact with the recording medium whenever the front latch is closed.

The magnetic head is positioned over the desired track by means of a 4-phase stepper motor/band assembly and its associated electronics. This positioner employs a one-step rotation to cause a 1-track linear movement. When a write-protected diskette is inserted into the Drive, the write-protect sensor disables the write electronics of the Drive and an appropriate signal is applied to the interface.

When performing a write operation, a 0.33 mm (0.013-in.) data track is recorded. This track is then tunnel erased to 0.30 mm (0.012-in.).

Data recovery electronics include a low-level read amplifier, differentiator, zero-crossing detector, and digitizing circuits. All data decoding is provided by the adapter card.

The Drive is also supplied with the following sensor systems:

- (1) A track 00 switch which senses when the Head/Carriage assembly is positioned at Track 00.
- (2) The index sensor, which consists of a LED light source and phototransistor, is positioned so that when an index hole is detected, a digital signal is generated.

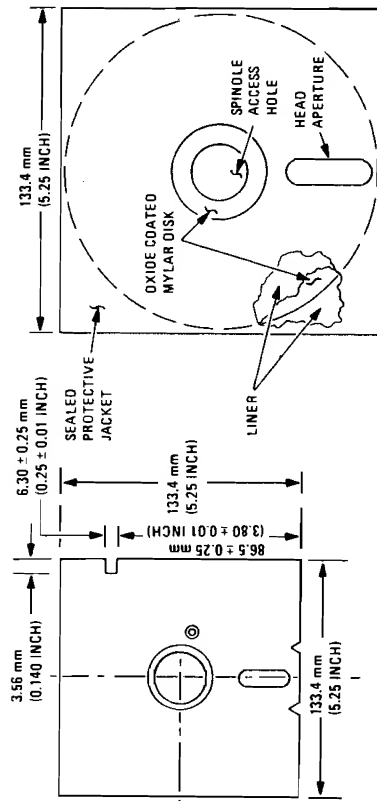
HARDWARE

- (3) The write-protect sensor disables the Diskette Drive electronics whenever a write-protect tab is applied to the diskette.

For interface information, refer to the Diskette Drive Adapter section.

Diskettes

The IBM 5-1/4" Diskette Drive uses a standard 133.4 mm (5.25 in.) diskette. For programming considerations, single sided, double density, soft sectored diskettes are used for single sided drives and double sided, double density, soft sectored diskettes are used for double sided drives. The figure below is a simplified drawing of the diskette used with the Diskette Drive. This recording medium is a flexible magnetic disk enclosed in a protective jacket. The protected disk, free to rotate within the jacket, is continuously cleaned by the soft fabric lining of the jacket during normal operation. Read/Write erase head access is made through an opening in the jacket. Openings for the drive hub and diskette index hole are also provided.



RECORDING MEDIUM

Table 18. Mechanical and Electrical Specifications

Media	Industry-compatible 5¼-inch diskette
Tracks per inch	48
Number of Tracks	(40)
Dimensions	
Height	85.85 mm (3.38 inches)
Width	149.10 mm (5.87 inches)
Depth	203.2 mm (8.0 inches)
Weight	2.04 Kg (4.5 lbs.)
Temperature (Exclusive of Media)	
Operating	10°C to 44°C (50°F to 112°F)
Non-operating	-40°C to 60°C (-40°F to 140°F)
Relative Humidity (Exclusive of Media)	
Operating	20% to 80% (Non-condensing)
Non-operating	5% to 95% (Non-condensing)
Seek Time	8 msec track to track
Head Setting Time	25 msec (last track addressed)
Error Rate	1 per 10 ⁹ (recoverable) 1 per 10 ¹² (non-recoverable) 1 per 10 ⁶ (seeks)
Head Life	20,000 hours (normal use)
Media Life	3.0 x 10 ⁶ passes per track
Disk Speed	300 rpm ± 1.5% (long term)
Instantaneous Speed Variation	± 3.0%
Start/Stop Time	500 msec (maximum)
Transfer Rate	250K bits/sec
Recording Mode	MFM
Power	+12 dc ± 0.6v 900 ma AVE. +5v dc ± 0.25 v, 600 ma AVE.

Memory Expansion Options

Three Memory Expansion Options are offered for the IBM Personal Computer. They are the 32KB, the 64KB, and the 64/256KB Memory Expansion Options. The base 64/256KB Option comes standard with 64KB of memory. One, two, or three 64KB Memory Module Kits may be added, providing the 64/256KB Option with 128KB, 192KB, or 256KB of memory respectively. The Memory Expansion Options plug into any of the five System Expansion Slots on the System Board and are used to extend system memory beyond 64KB. A maximum of 64KB of memory may be installed on the System Board as modules without using any System Expansion Slots or Expansion Options.

An expansion option must be configured to reside at a sequential 32K or 64K memory address boundary within the system address space. This is done by setting DIP switches on the option.

The expansion options are designed with 250 ns access dynamic memory chips. The 32KB and the 64KB options both use 16K x 1 memory chips while the 64/256KB option uses 64K x 1 memory chips. On the 32KB and the 64/256KB cards, 16 pin industry standard parts are used. On the 64KB card, stacked modules are used resulting in a 32K x 1, 18 pin module. This allows the 32KB and 64KB cards to have approximately the same physical dimensions.

All expansion options are parity checked and if a parity error is detected, a latch is set and an I/O channel check line is activated, indicating an error to the processor.

In addition to the memory modules, the expansion options contain the following circuits: bus buffering, dynamic memory timing generation, address multiplexing, and card select decode logic.

Dynamic memory refresh timing and address generation are functions which are not performed on the expansion options but are done once on the System Board and made available in the I/O channel for all devices.

To allow the System to address 32KB, 64KB, 64/256KB Memory Expansion Options, refer to the system configuration switch settings on page 2-28.

Operating Characteristics

The System Board operates at a frequency of 4.77 Mhz, which results in a clock frequency of 210 ns.

Normally, five clock cycles are required for a bus cycle so that a 1.05 μ s memory cycle time is achieved. Memory write and memory read cycles both take five clock cycles, or 1.05 μ s.

General specifications for memory used on all cards are:

Access - 250 ns
Cycle - 410 ns

Memory Module Description

Both the 32KB and 64KB options contain 18 dynamic memory modules. The 32KB Memory Expansion Option utilizes 16K x 1 bit modules and the 64KB Memory Expansion Option utilizes 32K x 1 bit modules.

The 64/256KB card has four banks of 9 pluggable connectors. Each bank will accept a 64KB Memory Module Kit, consisting of 9 (64K x 1) modules. The kits must be installed sequentially into Banks 1, 2, and 3. The base 64/256KB card comes standard with the first bank of modules installed into Bank 0, providing 64KB of memory. One, two, or three 64KB Kits may be added, upgrading the card to 128KB, 192KB, or 256KB of memory.

The 16K x 1 and the 32K x 1 modules require three voltage levels: +5 Vdc, -5 Vdc, and +12 Vdc. The 64K x 1 modules only require one voltage level of +5 Vdc. All three memory modules require 128 refresh cycles every 2 msec. Absolute maximum access times are:

From RAS: 250 ns
From CAS: 160 to 165 ns

Table 19. Memory Module Pin Configuration

PIN NO.	16K X 1 BIT MODULE (Used on 32KB Card)	32K X 1 BIT MODULE (Used on 64KB Card)	64K X 1 BIT MODULE (Used on 64/256KB Card)
1	-5V	-5V	N/C
2	Data In**	Data In**	Data In***
3	-Write	-Write	-Write
4	-RAS	-RAS 0	-RAS
5	A0	-RAS 1	A0
6	A2	A0	A2
7	A1	A2	A1
8	+12V	A1	+5VDC
9	+5V	+12V	A7
10	A5	+5V	A5
11	A4	A5	A4
12	A3	A4	A3
13	A6	A3	A6
14	Data Out**	A6	Data Out***
15	-CAS	Data Out**	-CAS
16	GND	-CAS 1	GND
17	-*	-CAS 0	.
18	-*	GND	.

* 16K X 1 and 64K X 1 bit module has only 16 pins.

** Data In and Data Out are tied together (three state bus).

*** Data In and Data Out are tied together on Data Bits 0-7 (three state bus).

Switch-Configurable Start Address

Each card has a small DIP Module which contains eight switches. The switches are used to set the card start address as follows:

Table 20. DIP Module Start Address

NO.	32KB AND 64KB OPTIONS	64/256KB OPTION
1	ON: A19=0; OFF: A19=1	ON: A19=0; OFF: A19=1
2	ON: A18=0; OFF: A18=1	ON: A18=0; OFF: A18=1
3	ON: A17=0; OFF: A17=1	ON: A17=0; OFF: A17=1
4	ON: A16=0; OFF: A16=1	ON: A16=0; OFF: A16=1
5	ON: A15=0; OFF: A15=1*	ON: Select 64KB
6	Not Used	ON: Select 128KB
7	Not Used	ON: Select 192KB
8	Used Only In 64KB RAM Card*	ON: Select 256KB

* Switch No. 8 may be set on the 64KB Memory Expansion. Option to use only half the memory on the card (i.e., 32KB). If Switch No. 8 is ON, all 64KB is accessible. If Switch No. 8 is OFF, address bit A15 (as set by Switch No. 5) is used to determine which 32KB are accessible and the 64KB option behaves exactly like a 32KB option.

Game Control Adapter

The Game Control Adapter allows the system to attach paddles and joysticks. Up to four paddles or two joysticks may be attached. In addition, four inputs for switches are provided. Paddle and joystick positions are determined by changing resistive values sent to the adapter. The adapter plus system software converts the present resistive value to a relative paddle or joystick position. On receipt of an output signal, four timing circuits are started. By determining the time required for the circuit to time out (a function of the resistance), the paddle position can be determined. This card could be used as a general purpose I/O card with four analog (resistive) inputs plus four digital input points. This card fits into any of the five System Board I/O slots. The game control interface cable attaches to the rear of the card which protrudes through the rear panel of the System Unit.

Game Control Adapter Block Diagram

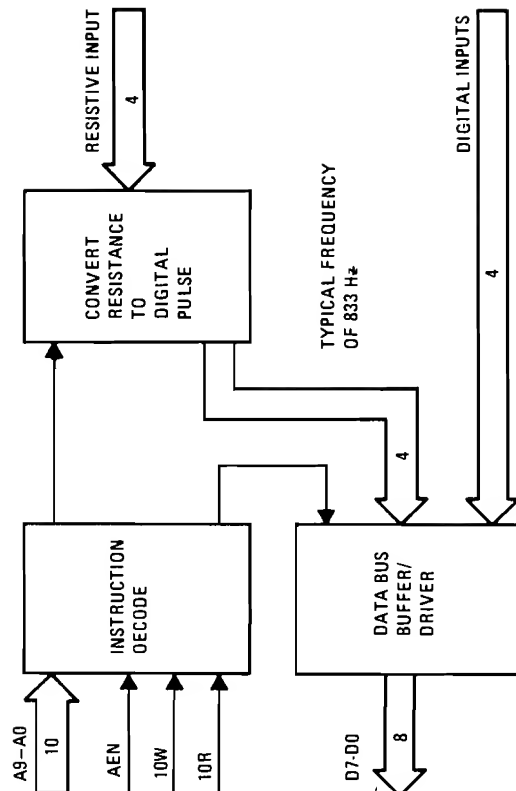


Figure 20. GAME CONTROL ADAPTER BLOCK DIAGRAM

Functional Description

Address Decode

The select on the Game Control Adapter is generated by two 74LS138's as an address decoder. AEN must be inactive while the address is 201 in order to generate the select. The select allows a write to fire the one-shots or a read to give the values of the trigger buttons and one-shot outputs.

Data Bus Buffer/Driver

The data bus is buffered by a 74LS244 buffer/driver. For an IN from address X'201', the Game Control Adapter will drive the data bus; at all other times the buffer is left in the high impedance state.

Trigger Buttons

The trigger button inputs are read via an IN from address X'201'. A trigger button is on each joystick/paddle. These values are seen on data bits 7 through 4 (see Software Interface sub-section). These buttons default to an open state and are read as "1". When a button is depressed, it is read as "0". Software should be aware that these buttons are NOT debounced in hardware.

Joystick Positions

The joystick position is indicated by a potentiometer for each coordinate. Each potentiometer has a range from 0 to 100K ohms that varies the time constant for each of the four one-shots. As this time constant is set at different values, the output of the one-shot will be of varying durations.

All four one-shots are fired at once by an OUT to address X'201'. All four one-shot outputs will go true after the fire pulse and will remain high for varying times depending on where each potentiometer is set.

These four one-shot outputs are read via an IN from address X'201' and are seen on data bits 3 through 0.

I/O Channel Description

A9-A0:	Address lines 9 through 0 are used to address the Game Control Adapter.
D7-D0:	Data lines 7 through 0 are the data bus.
IOR, IOW:	I/O Read and I/O Write are used when reading from or writing to an adapter (IN, OUT).
AEN:	When active, the adapter must be inactive and the data bus driver inactive.
+5V:	Power for the Game Control Adapter.
GND:	Common ground.
A19-A10:	Unused
MEMR, MEMW:	Unused
DACK0-DACK3:	Unused
IRQ7-IRQ2:	Unused
DRQ3-DRQ1:	Unused
ALE, T/C:	Unused
CLK, OSC:	Unused
I/O CHCK:	Unused
I/O CH RDY:	Unused
HRQ I/O CH:	Unused
RESET DRV:	Unused
-5V, +12V, -12V:	Unused

Interface Description

The Game Control Adapter has 8 input lines, 4 of which are digital inputs and 4 of which are resistive inputs. The inputs are read with one IN from address X'201'.

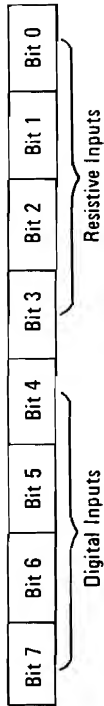
The 4 digital inputs each have a 1K ohm pullup resistor to +5V. With no drive on these inputs, a '1' is read. For a '0' reading, the inputs must be pulled to ground.

The 4 resistive inputs, measured to +5V, will be converted to a digital pulse with a duration proportional to the resistive load, according to the following equation:

$$\text{Time} = 24.2 \mu\text{sec} + 0.011 (r) \mu\text{sec}$$

The user must first begin the conversion by an OUT to address x'201'. An IN from address x'201' will show the digital pulse go high and remain high for the duration according to the resistance value. All four bits (Bit 3-Bit 0) function in the same manner, their digital pulse will all go high simultaneously and will reset independently according to the input resistance value.

Input from address x'201'



The typical input to the Game Control Adapter is a set of joysticks or game paddles.

The joysticks will typically have a set of two joysticks (A&B). These will have one or two buttons each with two variable resistances each, with a range from 0 to 100K ohms. One variable resistance will indicate the X coordinate and the other variable resistance will indicate the Y coordinate. This should be attached to give the following input data:

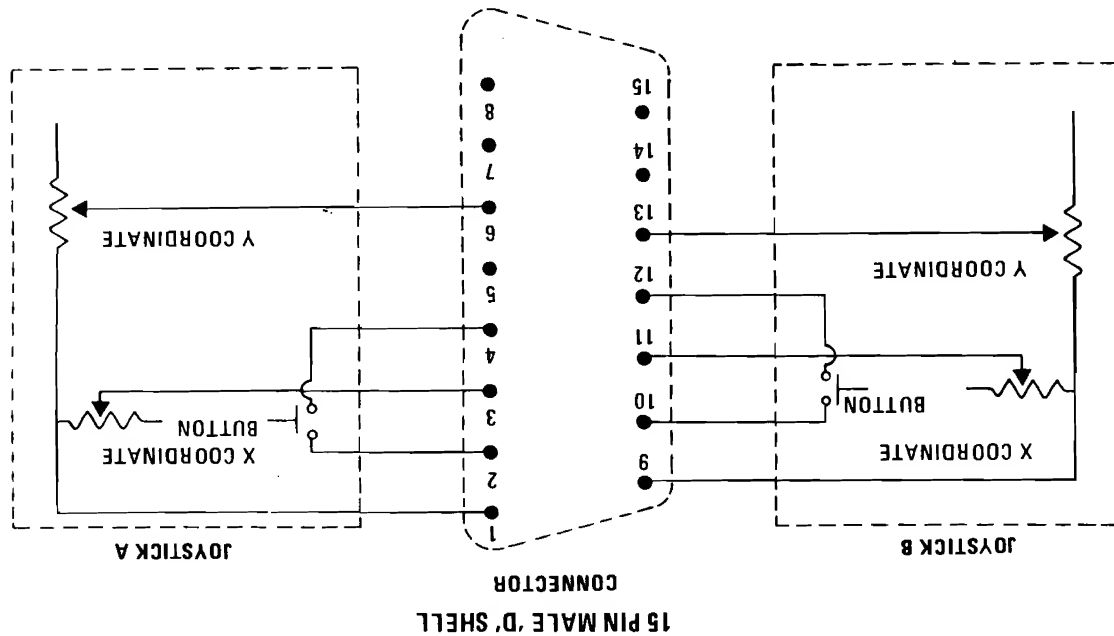
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B-#2 Button	B-#1 Button	A-#2 Button	A-#1 Button	B-Y Coord.	B-X Coord.	A-Y Coord.	A-X Coord.

The game paddles will have a set of two (A&B) or four (A,B,C, & D) paddles. These will have one button each and one variable resistance each, with a range from 0 to 100K ohms. This should be attached to give the following input data:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D Button	C Button	B Button	A Button	D Coord.	C Coord.	B Coord.	A Coord.

A schematic diagram for attaching a set of game controllers is on page 2-135.

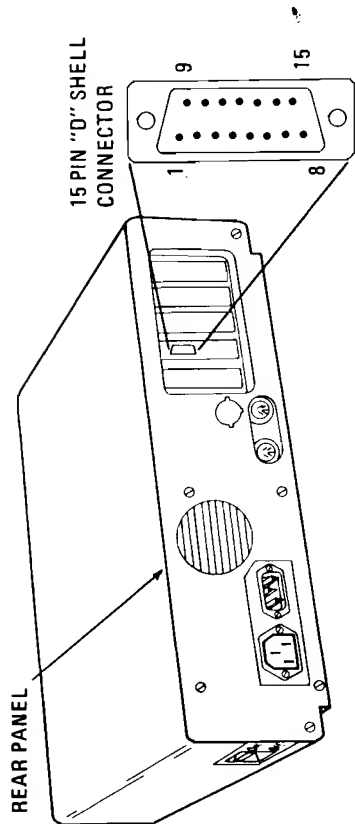
Joystick Schematic



NOTE: POTENTIOMETER FOR X & Y COORDINATES HAS A RANGE OF 0 TO 100KΩ.
BUTTON IS NORMALLY OPEN; CLOSED WHEN DEPRESSED.

Figure 21. JOYSTICK SCHEMATIC

Game Controller Adapter (Analog Input) Connector Specifications



AT STANDARD TTL LEVELS

Voltage	AMP	Pin No.
+ 5 Volts	Button 4	1
Position 0		2
Ground		3
Ground		4
Position 1		5
Button 5		6
+ 5 Volts		7
+ 5 Volts		8
Button 6		9
Position 2		10
Ground		11
Position 3		12
Button 7		13
+ 5 Volts		14
		15

External Devices

Game Control Adapter

Asynchronous Communications Adapter

The Asynchronous Communications Adapter is a 4"H x 5"W card that plugs into a System Expansion Slot. All system control signals and voltage requirements are provided through a 2 x 31 position card edge tab. A jumper module is provided to select either RS-232-C or current loop operation.

The adapter is fully programmable and supports asynchronous communications only. It will add and remove start bits, stop bits, and parity bits. A programmable baud rate generator allows operation from 50 baud to 9600 baud. Five, six, seven or eight bit characters with 1, 1-1/2, or 2 stop bits are supported. A fully prioritized interrupt system controls transmit, receive, error, line status and data set interrupts. Diagnostic capabilities provide loopback functions of transmit/receive and input/output signals.

Figure (22) is a block diagram of the Asynchronous Communications Adapter.

The heart of the adapter is a INS8250 LSI chip or functional equivalent. The following is a summary of the 8250's key features:

- Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop, and Parity) to or from Serial Data Stream.
- Full Double Buffering Eliminates Need for Precise Synchronization.
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts.
- Programmable Baud Rate Generator Allows Division of Any Input Clock by 1 to ($2^{16}-1$) and Generates the Internal 16x Clock.
- Independent Receiver Clock Input.
- MODEM Control Functions – Clear to Send (CTS), Request to Send (RTS), Data Set Ready (DSR), Data Terminal Ready (DTR), Ring Indicator (RI), and Carrier Detect (CD).
- Fully Programmable Serial-Interface Characteristics
 - 5-, 6-, 7-, or 8-Bit Characters
 - Even, Odd, or No-Parity Bit Generation and Detection
 - 1-, 1-1/2, or 2-Stop Bit Generation
 - Baud Rate Generation (DC to 9600 Baud)

- False Start Bit Detection.
- Complete Status Reporting Capabilities.
- Line Break Generation and Detection.
- Internal Diagnostic Capabilities.
 - Loopback Controls for Communications Link Fault Isolation.
 - Break, Parity, Overrun, Framing Error Simulation.
- Full Prioritized Interrupt System Controls.

All communications protocol is a function of the system micro-code and must be loaded before the adapter is operational. All pacing of the interface and control signal status must be handled by the system software.

Asynchronous Communications Block Diagram

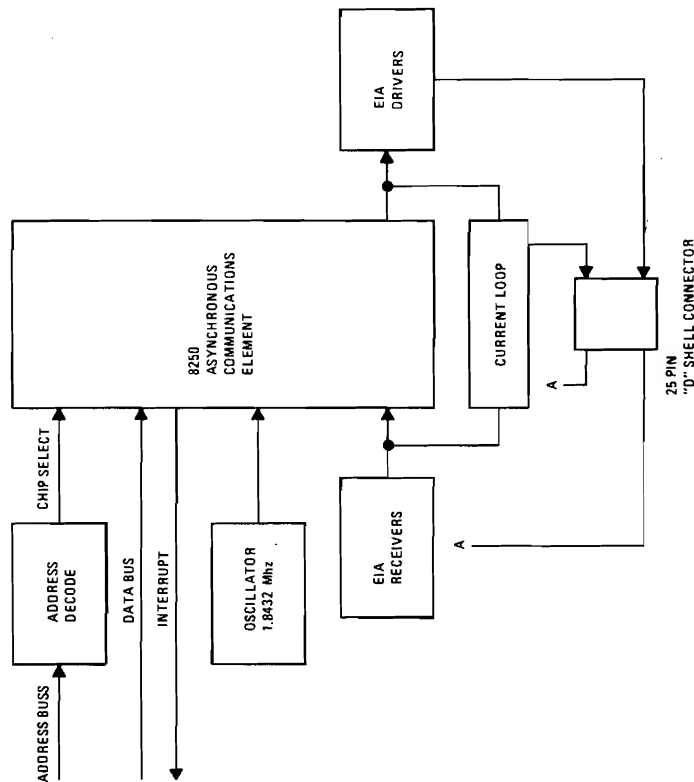


Figure 22. ASYNCHRONOUS COMMUNICATIONS ADAPTER BLOCK DIAGRAM

Modes of Operation

The different modes of operation are selected by programming the 8250 Asynchronous Communications Element. This is done by selecting the I/O address (3F8 to 3FF) and writing data out to the card. Address bit A0, A1 and A2 select the different registers which define the modes of operation. Also, the Divisor Latch Access Bit (Bit 7) of the line control register is used to select certain registers.

I/O Decode for Communications Adapter

Table 21. I/O Decodes (3F8 - 3FF)

I/O DECODE	REGISTER SELECTED	DLAB STATE
3F8	TX BUFFER	DLAB=0 (WRITE)
3F8	RX BUFFER	DLAB=0 (READ)
3F8	DIVISOR LATCH LSB	DLAB=1
3F9	DIVISDR LATCH MSB	DLAB=1
3F9	INTERRUPT ENABLE REGISTER	DLAB=0
3FA	INTERRUPT IDENTIFICATION REGISTERS	
3FB	LINE CONTROL REGISTER	
3FC	MODEM CONTROL REGISTER	
3FD	LINE STATUS REGISTER	
3FE	MODEM STATUS REGISTER	

ADDRESS BITS

	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	DLAB	REGISTER
3F8 to 3FF	1	1	1	1	1	1	1	1	0	0	0	Receive Buffer (read), Transmrit Holding Reg. (write)
								0	0	1	0	Interrupt Enable
								0	1	0	X	Interrupt Identification
								0	1	1	X	Line Control
								1	0	0	X	Modem Control
								1	1	0	1	Line Status
								1	1	1	0	Modem Status
								0	0	0	X	None
								0	0	1	X	Divisor Latch (LSB)
								0	0	1	1	Divisor Latch (MSB)

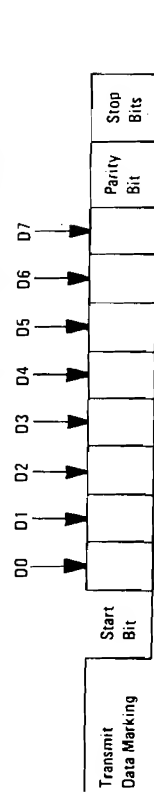
A2, A1 and A0 bits are "Don't Cares" and are used to select the different register of the communications chip.

Interrupts

One interrupt line is provided to the system. This interrupt is IRQ4 and will be positive active. To allow the communications card to send interrupts to the system, Bit 3 of the Modem Control Register must be set = 1 (high). At this point, any interrupts allowed by the Interrupt Enable Register will cause an interrupt.

The data format will be as follows:

TRANSMITTER OUTPUT AND RECEIVER INPUT



Data Bit 0 is the first bit to be transmitted or received. The adapter automatically inserts the start bit, the correct parity bit if programmed to do so, and the stop bit (1, 1-1/2 or 2 depending on the command in the Line Control Register).

Interface Description

The communications adapter provides an EIA RS-232-C, or equivalent, interface. One 25 pin "D" shell, male type connector is provided to attach various peripheral devices. In addition, a current loop interface is also located in this same connector. A jumper block is provided to manually select either the voltage interface, or the current loop interface.

- Pin 18 + receive current loop data (20Ma)
- Pin 25 - receive current loop return (20Ma)
- Pin 9 + transmit current loop return (20Ma)
- Pin 11 - transmit current loop data (20Ma)

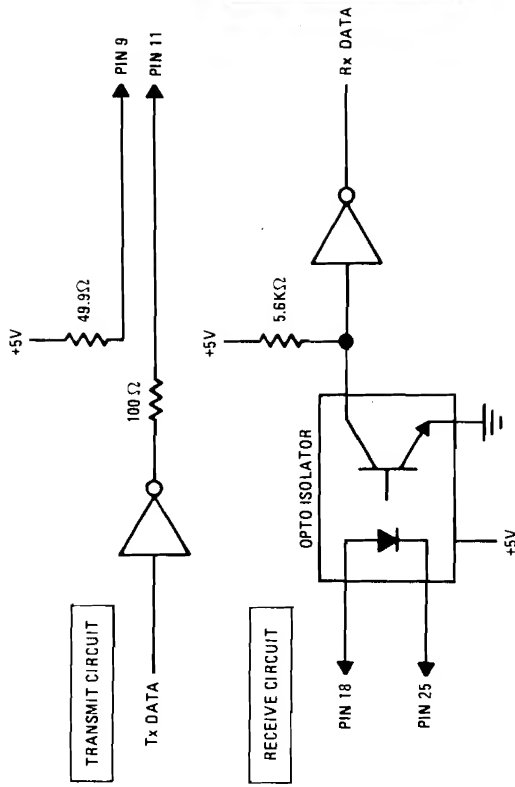


Figure 23. CURRENT LOOP INTERFACE

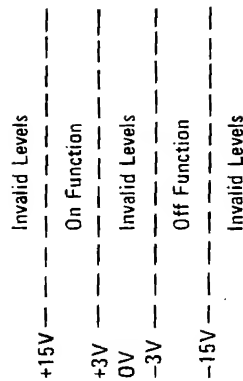
The voltage interface is a serial interface. It supports certain data and control signals as listed below:

- Pin 2 Transmit Data
- Pin 3 Receive Data
- Pin 4 Request to Send
- Pin 5 Clear to Send
- Pin 6 Data Set Ready
- Pin 7 Signal Ground
- Pin 8 Carrier Detect
- Pin 20 Data Terminal Ready
- Pin 22 Ring Indicate

The adapter converts these signals from TTL to EIA voltage levels and from EIA to TTL voltage levels. These signals are sampled or generated by the communication control chip. These signals can then be sensed by the system software to determine the state of the interface or peripheral device.

Voltage Interchange Information

Interchange Voltage	Binary State	Signal Condition	Interface Control Function
Positive Voltage =	Binary (0)	= Spacing	=On
Negative Voltage =	Binary (1)	= Marking	=Off



The signal will be considered in the "marking" condition when the voltage on the interchange circuit, measured at the interface point, is more negative than minus three volts with respect to signal ground. The signal will be considered in the "spacing" condition when the voltage is more positive than plus three volts with respect to signal ground. The region between plus three volts and minus three volts is defined as the transition region and is considered an invalid level. The voltage which is more negative than -15V or more positive than +15V will be considered in invalid levels.

During the transmission of data, the "marking" condition will be used to denote the binary state "one" and "spacing" condition will be used to denote the binary state "zero".

For interface control circuits, the function is "on" when the voltage is more positive than +3V with respect to signal ground and is "off" when the voltage is more negative than -3V with respect to signal ground.

INS8250 Functional Pin Description

The following describes the function of all INS8250 input/output pins. Some of these descriptions reference internal circuits.

Note: In the following descriptions, a low represents a logic 0 (0 volt nominal) and a high represents a logic 1 (+2.4 volts nominal).

Input Signals

Chip Select (CS0, CS1, CS2), Pins 12-14: When CS0 and CS1 are high and CS2 is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) Address Strobe (ADS) input. This enable communication between the INS8250 and the CPU.

Data Input Strobe (DISTR, $\overline{\text{DISTR}}$) Pins 22 and 21: When DISTR is high or $\overline{\text{DISTR}}$ is low while the chip is selected, allows the CPU to read status information or data from a selected register of the INS8250.

Note: Only an active DISTR or $\overline{\text{DISTR}}$ input is required to transfer data from the INS8250 during a read operation. Therefore, tie either the DISTR input permanently low or the DISTR input permanently high, if not used.

Data Output Strobe (DOSTR, $\overline{\text{DOSTR}}$), Pins 19 and 18: When DOSTR is high or $\overline{\text{DOSTR}}$ is low while the chip is selected, allows the CPU to write data or control words into a selected register of the INS8250.

Note: Only an active DOSTR or $\overline{\text{DOSTR}}$ input is required to transfer data to the INS8250 during a write operation. Therefore, tie either the DOSTR input permanently low or the DOSTR input permanently high, if not used.

Address Strobe (ADS), Pin 25: When low, provides latching for the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, CS2) signals.

Note: An active ADS input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the ADS input permanently low.

Register Select (A0, A1, A2), Pins 26-28: These three inputs are used during a read or write operation to select an INS8250 register to read from or write into as indicated in the table below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain INS8250 registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

DLAB	A2	A1	A0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	None
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Master Reset (MR), Pin 35: When high, clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the INS8250. Also, the state of various output signals (SOUT, INTRPT, OUT 1, OUT 2, RTS, DTR) are affected by an active MR input. (Refer to Table 1.)

Receiver Clock (RCLK), Pin 9: This input is the 16x baud rate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, MODEM, or data set).

Clear to Send (CTS), Pin 36: The CTS signal is a MODEM control function input whose condition can be tested by the CPU by reading Bit 4 (CTS) of the MODEM Status Register. Bit 0 (DCTS) of the MODEM Status Register indicates whether the CTS input has changed state since the previous reading of the MODEM Status Register.

Note: Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Data Set Ready (DSR), Pin 37: When low, indicates that the MODEM or data set is ready to establish the communications link and transfer data with the INS8250. The DSR signal is a MODEM-control function input whose condition can be tested by the CPU by reading Bit 5 (DSR) of the MODEM Status Register. Bit 1 (DDSR) of the MODEM Status Register indicates whether the DSR input has changed state since the previous reading of the MODEM Status Register.

Note: Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Received Line Signal Detect (RLSD), Pin 38: When low, indicates that the data carrier has been detected by the MODEM or data set. The RLSD signal is a MODEM-Control function input whose condition can be tested by the CPU by reading Bit 7 (RLSD) of the MODEM Status Register. Bit 3 (DRLSD) of the MODEM Status Register indicates whether the RLSD input has changed state since the previous reading of the MODEM Status Register.

Note: Whenever the RLSD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Ring Indicator (RI), Pin 39: When low, indicates that a telephone ringing signal has been received by the MODEM or data set. The RI signal is a MODEM-control function input whose condition can be tested by the CPU by reading Bit 6 (RI) of the MODEM Status Register. Bit 2 (TERI) of the MODEM Status Register indicates whether the RI input has changed from a low to a high state since the previous reading of the MODEM Status Register.

Note: Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Interrupt is enabled.

VCC, Pin 40: +5 volt supply.

VSS, Pin 20: Ground (0-volt) reference.

Output Signals

Data Terminal Ready (DTR), Pin 33: When low, informs the MODEM or data set that the INS8250 is ready to communicate. The DTR output signal can be set to an active low by programming Bit 0 (DTR) of the MODEM Control Register to a high level. The DTR signal is set high upon a Master Reset operation.

Request to Send (RTS), Pin 32: When low, informs the MODEM or data set that the INS8250 is ready to transmit data. The RTS output signal can be set to an active low by programming Bit 1 (RTS) of the MODEM Control Register. The RTS signal is set high upon a Master Reset operation.

Output 1 (OUT 1), Pin 34: User-designated output that can be set to an active low by programming Bit 2 (OUT 1) of the MODEM Control Register to a high level. The OUT 1 signal is set high upon a Master Reset operation.

Output 2 (OUT 2), Pin 31: User-designated output that can be set to an active low by programming Bit 3 (OUT 2) of the MODEM Control Register to a high level. The OUT 2 signal is set high upon a Master Reset operation.

Chip Select Out (CSOUT), Pin 24: When high, indicates that the chip has been selected by active CS0, CS1, and CS2 inputs. No data transfer can be initiated until the CSOUT signal is a logic 1.

Driver Disable (DDIS), Pin 23: Goes low whenever the CPU is reading data from the INS8250. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and INS8250 on the D7-D0 Data Bus) at all times, except when the CPU is reading data.

Baud Out (BAUDOUT), Pin 15: 16x clock signal for the transmitter section of the INS8250. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The BAUDOUT may also be used for the receiver section by typing this output to the RCLK input of the chip.

Interrupt (INTRPT), Pin 30: Goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag; Received Data Available; Transmitter Holding Register Empty; and MODEM Status. The INTRPT Signal is reset low upon the appropriate interrupt service or a Master Reset operation.

Serial Output (SOUT), Pin 11: Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (Logic 1) state upon a Master Reset operation.

Input/Output Signals

Data (D7-D0) Bus, Pins 1-8: This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the INS8250 and the CPU. Data, control words, and status information are transferred via the D7-D0 Data Bus.

External Clock Input/Output (XTAL1, XTAL2, Pins 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the INS8250.

Programming Considerations

Table 22. Asynchronous Communications Reset Functions

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All Bits Low (0-3 Forced and 4-7 Permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3-7 are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	Except Bits 5 & 6 are High
MODEM Status Register	Master Reset	Bits 0-3 Low Bits 4-7 - Input Signal
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (RCVR Data Ready)	Read IIR/Write THR/MR	Low
INTRPT (MODEM Status Changes)	Read MSR/MR	Low
OUT 2	Master Reset	High
RTS	Master Reset	High
DTR	Master Reset	High
OUT 1	Master Reset	High

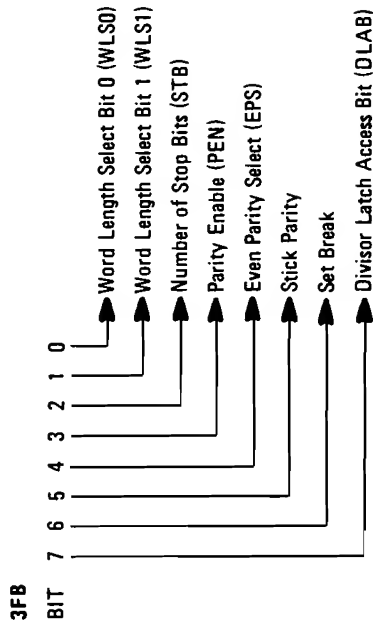
INS8250 Accessible Registers

The system programmer may access or control any of the INS8250 registers via the CPU. These registers are used to control INS8250 operations and to transmit and receive data.

INS8250 Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are indicated and described below.

Line Control Register (LCR)



Bit 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is logic 1 when a 5-bit word length is selected via bits 0 and 1, 1-1/2 Stop bits are generated or checked. If bit 2 is logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1's when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1's is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver as a logic 0 if bit 4 is a logic 1 or as a logic 1 if bit 4 is a logic 0.

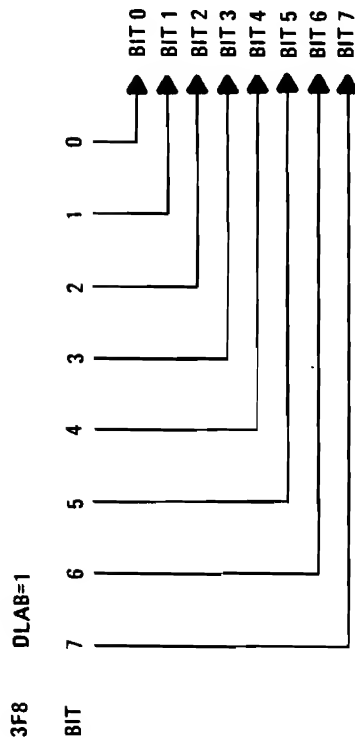
Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there regardless of other transmitter activity. The set break is disabled by setting bit 6 to a logic 0. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

INS8250 Programmable Baud Rate Generator

The INS8250 contains a programmable Baud Rate Generator that is capable of taking the clock input (1.8432 Mhz) and dividing it by any divisor from 1 to $(2^{16}-1)$. The output frequency of the Baud Rate Generator is $16 \times \text{Baud rate} [\text{divisor} \# = (\text{frequency input}) / (\text{baud rate} \times 16)]$. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Divisor Latch Least Significant Bit (DLL)



Divisor Latch Most Significant Bit (DLM)

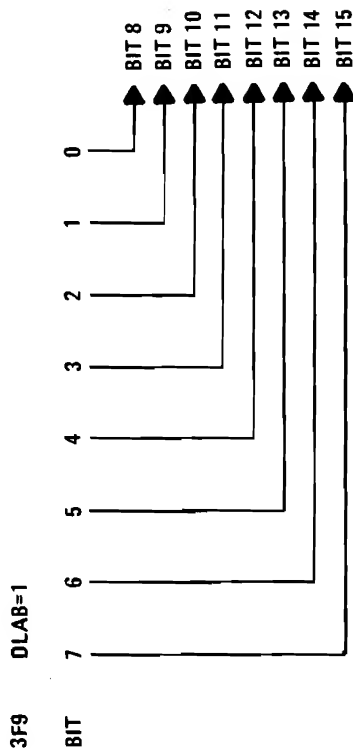


Table 23 illustrates the use of the Baud Rate Generator with a frequency of 1.8432 Mhz. For baud rates of 9600 and below, the error obtained is minimal.

Note: The maximum operating frequency of the Baud Generator is 3.1 Mhz. In no case should the data rate be greater than 9600 Baud.

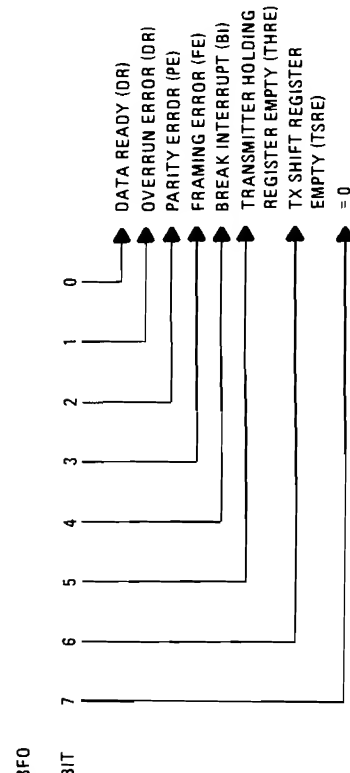
Table 23. BAUD Rate at 1.843 Mhz

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired & Actual
50	Decimal 2304 Hex '900'	---
75	1536 '600'	---
110	1047 '417'	---
134.5	857 '359'	0.026
150	768 '300'	0.058
300	384 '180'	---
600	192 '0C0'	---
1200	96 '060'	---
1800	64 '040'	---
2000	58 '03A'	0.89
2400	48 '030'	---
3600	32 '020'	---
4800	24 '018'	---
7200	16 '010'	---
9600	12 '00C'	---

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated and described below.

Line Status Register (LSR)



Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 may be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits).

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the INS8250 is ready to accept a new character for transmission. In addition, this bit causes the INS8250 to issue an interrupt to the CPU when the Transmitter Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon a data transfer from the Transmitter Holding Register to the Transmitter Shift Register. Bit 6 is a read-only bit.

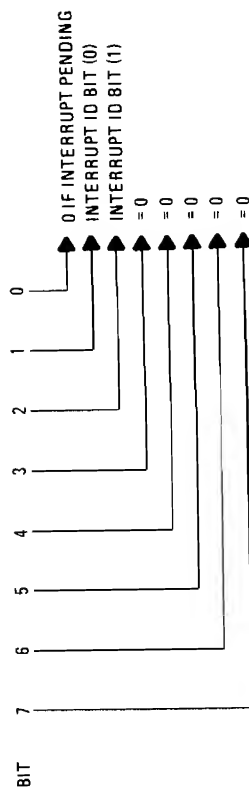
Interrupt Identification Register

The INS8250 has an on-chip interrupt capability that allows for complete flexibility in interfacing to all the popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the INS8250 prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and the type of that interrupt are stored in the Interrupt Identification Register (refer to Table 5). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until that particular interrupt is serviced by the CPU. The contents of the IIR are indicated and described below.

Interrupt Identification Register (IIR)

3FA



Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continued.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 5.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Table 24. Interrupt Control Functions (Asynchronous)

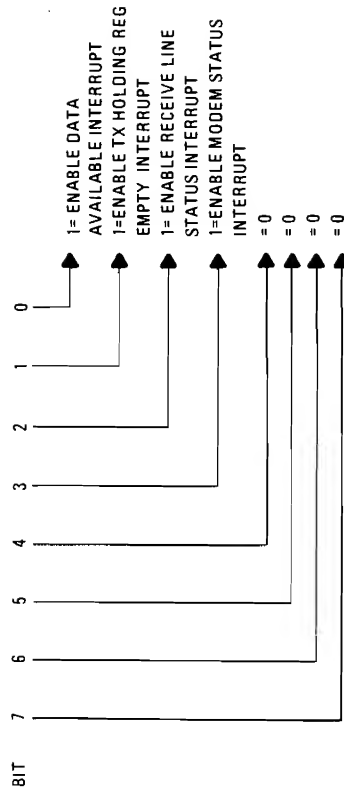
Interrupt ID Register				Interrupt Set and Reset Functions		
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

Interrupt Enable Register

This 8-bit register enables the four types of interrupt of the INS8250 to separately activate the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated and described below.

Interrupt Enable Register (IER)

3F9 DLAB=0



Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

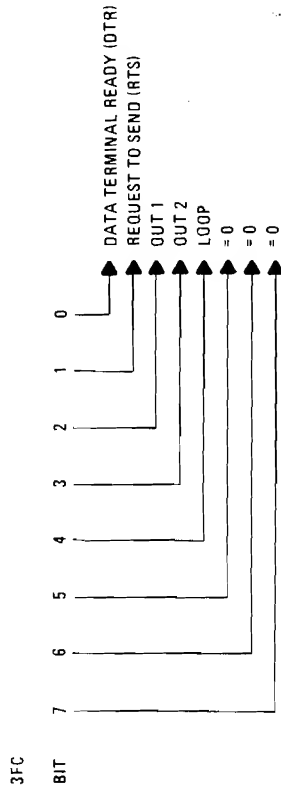
Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

MODEM Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated and described below.

MODEM Control Register (MCR)



Bit 0: This bit controls the Data Terminal Ready (DTR) output. When bit 0 is set to a logic 1, the DTR output is forced to a logic 0. When bit 0 is reset to a logic 0, the DTR output is forced to a logic 1.

Note: The DTR output of the INS8250 may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send (RTS) output. Bit 1 affects the RTS output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 (OUT 1) signal, which is an auxiliary user-designated output. Bit 2 affects the OUT 1 output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 (OUT 2) signal, which is an auxiliary user-designated output. Bit 3 affects the OUT 2 output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a loopback feature for diagnostic testing of the INS8250. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs (CTS, DSR, RLSD, and RI) are disconnected; and the four MODEM Control outputs (DTR, RTS, OUT 1, and OUT 2) are internally connected to the four MODEM Control inputs. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the INS8250.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The INS8250 interrupt system can be tested by writing into the lower four bits of the MODEM Status Register. Setting any of these bits to a logic 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal INS8250 operation. To return to normal operation, the registers must be reprogrammed for normal operation and then bit 4 of the MODEM Control Register must be reset to logic 0.

Bits 5 through 7: These bits are permanently set to logic 0.

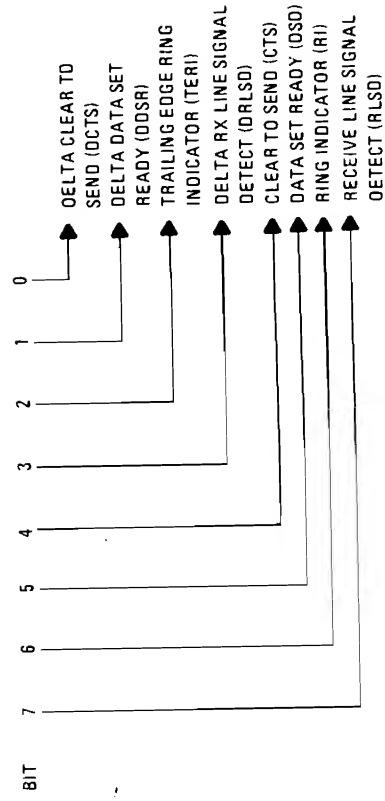
MODEM Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The content of the MODEM Status Register are indicated and described below.

MODEM Status Register (MSR)

3FE



Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the CTS input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator.

Bit 1 indicates that the DSR input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the RI input to the chip has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the RLSD input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to a logic 1, a MODEM Status interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send (CTS) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready (DSR) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

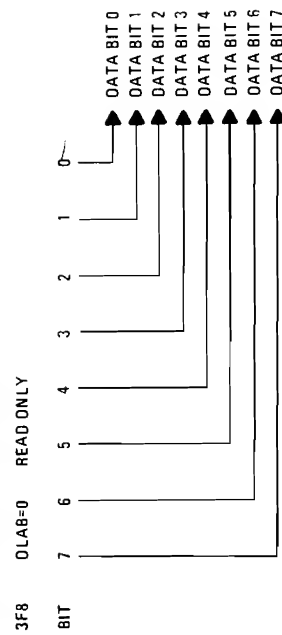
Bit 6: This bit is the complement of the Ring Indicator (RI) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the Received Line Signal Detect (RLSD) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 of the MCR.

Receiver Buffer Register

The Receiver Buffer Register contains the received character as defined below.

Receiver Buffer Register (RBR)

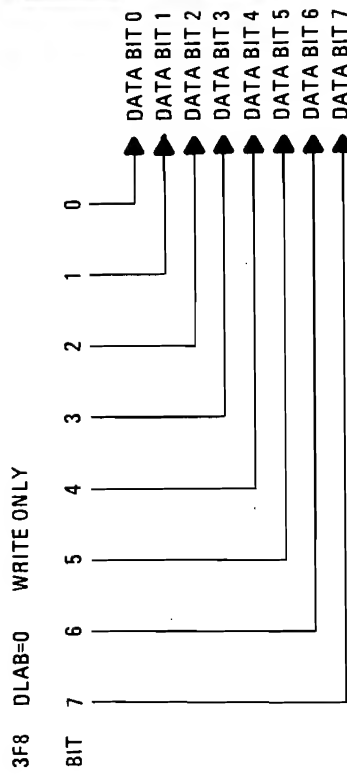


Bit 0 is the least significant bit and is the first bit serially received.

Transmitter Holding Register

The Transmitter Holding Register contains the character to be serially transmitted and is defined below:

Transmitter Holding Register (THR)



Bit 0 is the least significant bit and is the first bit serially transmitted.

Selecting the Interface Format and Adapter Address

The Voltage or Current loop interface and Adapter Address are selected by plugging the programmed shunt modules with the locator dots up or down. See the figure below for the configurations.

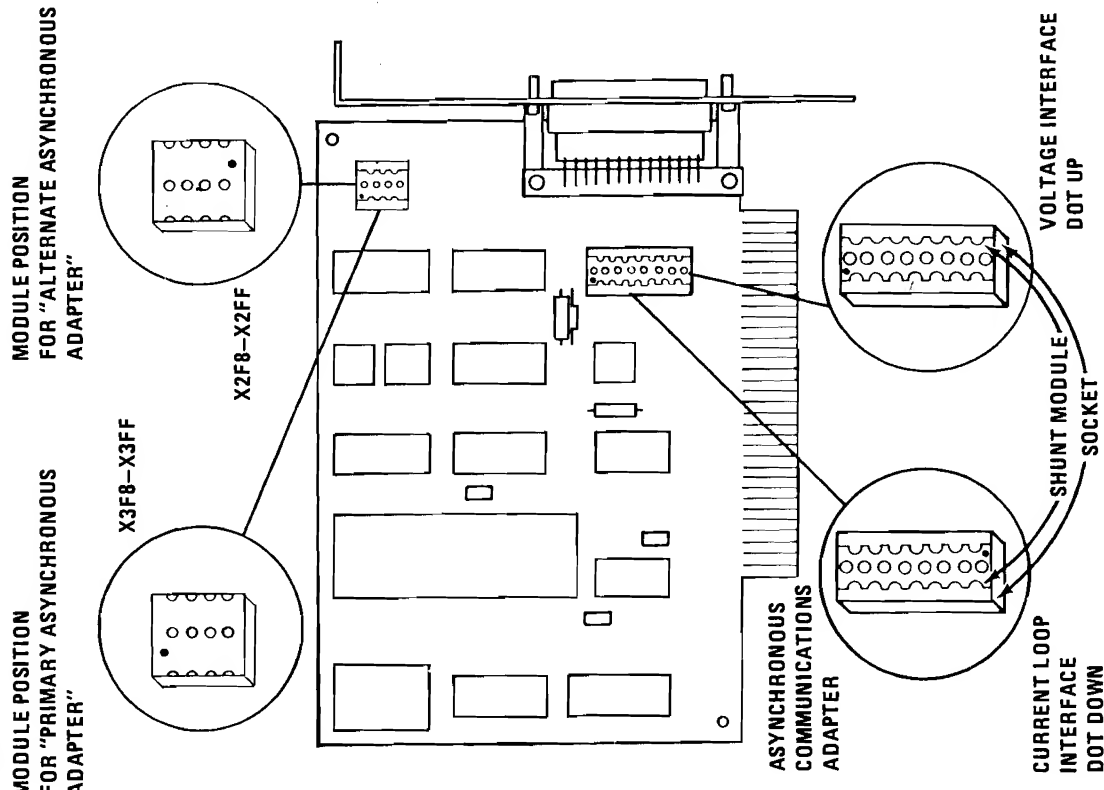
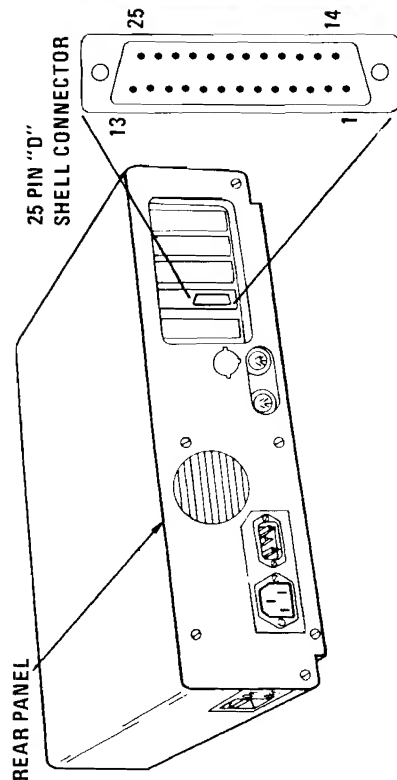


Figure 23. SELECTING THE INTERFACE FORMAT AND ADAPTER ADDRESS

Asynchronous Communications Adapter Connector Interface Specifications



HARDWARE

AT STANDARD TTL LEVELS

Pin	Description
1	NC
2	Transmit Data
3	Receive Data
4	Request to send
5	Clear to send
6	Data set ready
7	Signal ground
8	Carrier detect
9	+Transmit current loop return (20 ma)
10	NC
11	-Transmit current loop data (20 ma)
12	NC
13	NC
14	NC
15	NC
16	NC
17	NC
18	+Receive current loop data (20 ma)
19	NC
20	Data Terminal Ready
21	NC
22	Ring Indicate
23	NC
24	NC
25	-Receive current loop return (20 ma)

NOTE: To avoid inducing voltage surges on interchange circuits, signals from interchange circuits shall not be used to drive inductive devices, such as relay coils.

Prototype Card

The Prototype Card is 4.2 inches high x 13.2 inches long and plugs into a System Expansion Slot. All system control signals and voltage requirements are provided through a 2 x 31 position card edge tab.

The card contains a voltage bus (+5V) and a ground bus (0V). Each bus borders the card, with the voltage bus on the back (pin side) and the ground bus on the front (component side). A system interface design is also provided on the Prototype Card. The logic diagram for this interface is provided in Appendix D. The Prototype Card can also accommodate a D shell connector if it is needed. The connector size can range from a 9 to a 37 position connector.

Note: Install all components on the component side of the Prototype Card. The total width of the card including components should not exceed 0.700". If these specifications are not met, components on the Prototype Card may touch other cards plugged into adjacent slots.

Prototype Card Block Diagram

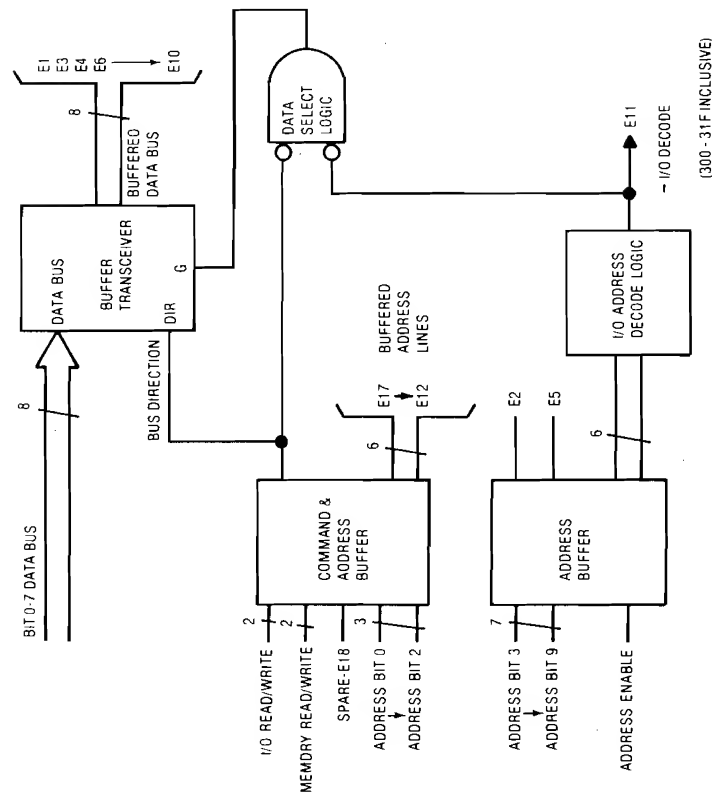


Figure 25. PROTOTYPE CARD BLOCK DIAGRAM

I/O Channel Interface

The Prototype Card has two layers screened onto it (one on the front and one on the back). It also has 3,909 plated through holes that are .040" in size and have a .060" pad which are located on a 0.10" grid. There are 37 plated through holes that are .048" in size. These holes are located at the rear of the card (viewed as if installed in the machine). These 37 holes are used for a 9 to 37 position D shell connector. The card also has 5 holes that are 0.125" in size. One hole is located just above the two rows of D shell connector holes, and the other four are located in the corners of the board (one in each corner).

Prototype Card Layout

The component side has the ground bus (.050" wide) screened on it and card edge tabs that are labeled A1 through A31.

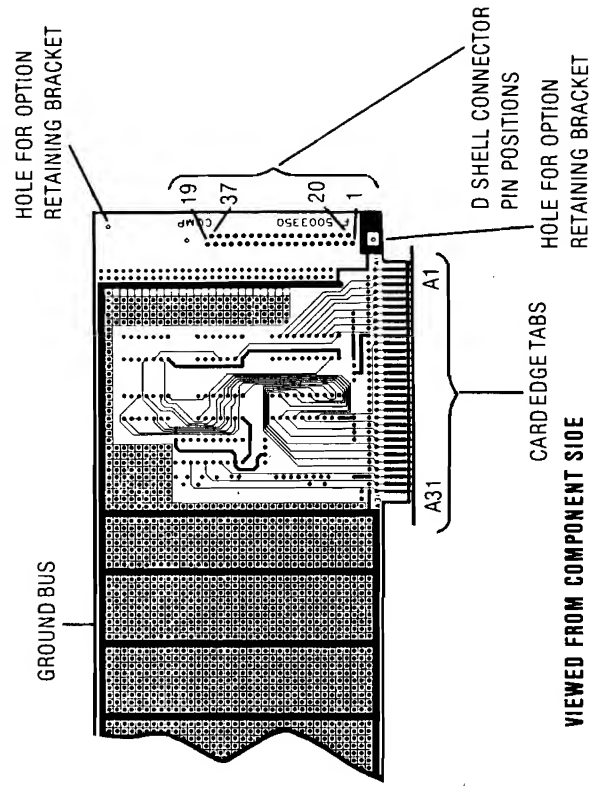
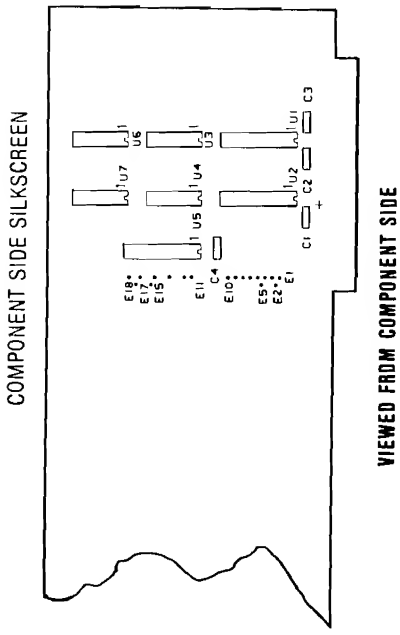


Figure 26. I/O CHANNEL INTERFACE

The component side also has a silk screen printed on it that is used as a component guide for the I/O interface.



The pin side has a voltage bus (+5v and .050" wide) screened onto it and card edge tabs that are labeled B1 through B31.

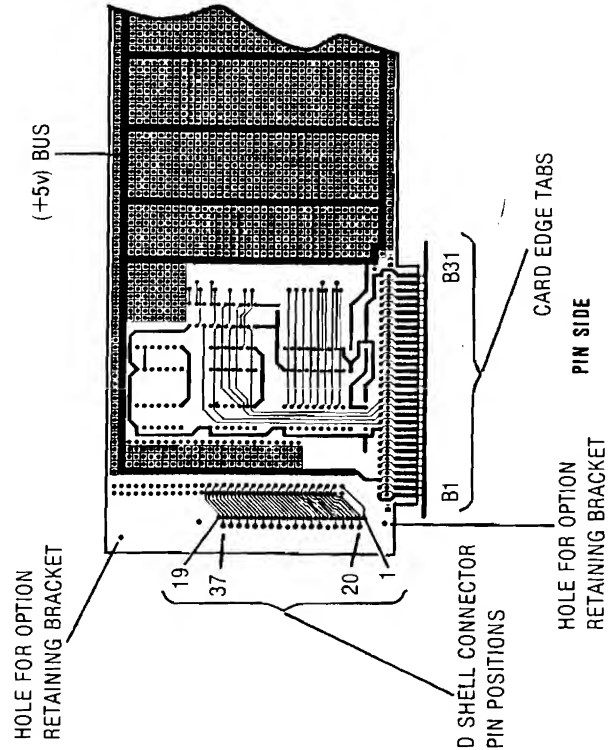


Figure 27. I/O CHANNEL INTERFACE

HARDWARE

Each card edge tab is connected to a plated through hole by a .012" land. There are three ground tabs connected to the ground bus by three .012" lands. Also, there are two +5V tabs connected to the voltage bus by two .012" lands.

Prototype Card to System Board Interface

The I/O Channel Description and I/O Channel Diagram are on pages 2-8 through 2-12 of this manual. Also the Prototype Card Interface Logic Diagram is in Appendix D page D-56. If the recommended interface logic is used, the list of TTL type numbers listed below will help you select the necessary components.

Component	TTL Number	Description
U1	74LS245	Octal Bus Transceiver
U2,U5	74LS244	Octal Buffers Line Driver/Line Receivers
U4	74LS04	Hex Inverters
U3	74LS08	Quadruple 2 - Input Positive - And Gate
U6	74LS02	Quadruple 2 - Input Positive - Nor Gate
U7	74LS21	Dual 4 - Input Positive - And Gate
C1		10.0 uf Tantalum Capacitor
C2,C3,C4		.047 uf Ceramic Capacitor

System Loading and Power Limitations

Because of the number of options that may be installed in the Personal Computer, the I/O bus loading should be limited to one Schottky TTL load. If the interface circuitry on the card is used, then this requirement is met.

The power limitations to be observed are located on pages 2-43 through 2-46 of this manual.

Prototype Card External Interface

If a connector is required for the card function, then you should purchase one of the recommended connectors (manufactured by Amp) or equivalent listed below:

HARDWARE	
Connector Size	Part Number (Amp)
9 pin D shell (Male)	205865-1
9 pin D shell (Female)	205866-1
15 pin D shell (Male)	205867-1
15 pin D shell (Female)	205868-1
25 pin D shell (Male)	205857-1
25 pin D shell (Female)	205858-1
37 pin D shell (Male)	205859-1
37 pin D shell (Female)	205860-1

EXAMPLE

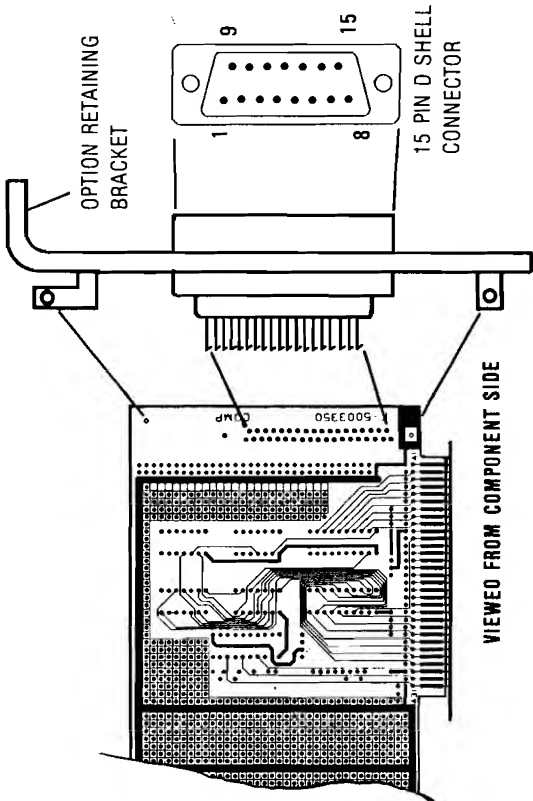


Figure 28. PROTOTYPE CARD EXTERNAL INTERFACE

SECTION 3. ROM and SYSTEM
USAGE

Contents

ROM BIOS 3-2

BIOS Cassette Logic 3-8

Keyboard Encoding and Usage 3-11

Low Memory Maps 3-21

ROM

ROM BIOS

The ROM resident Basic I/O System (BIOS) provides the device level control of the major I/O devices in the System Unit. The BIOS routines allow the assembly language programmer to perform block (diskette and cassette) or character (Video, communications, keyboard and printer) level I/O operations without any concern for device address and operating characteristics. Additionally, system services such as time of day and memory size determination are provided. The goal is to provide an operational interface to the system and relieve the programmer from concern over hardware device characteristics.

Finally the BIOS interface insulates the user from the hardware allowing new devices to be added to the System Unit, yet retaining the BIOS level interface to the device. In this manner, user programs become transparent to hardware modifications and enhancements. A complete listing of the BIOS is provided in Appendix "A".

Use of BIOS

Access to the BIOS function is through the 8088 software interrupts. Each BIOS entry point is available through its own interrupt, which can be found in the interrupt vector listing. The software interrupts 10H through 1AH each access a different BIOS routine. For example, to determine the amount of memory available in the system,

```
INT 12H
```

will invoke the memory size determination routine in BIOS and return the value to the caller.

Parameter Passing

All parameters passed to and from the BIOS routines go through the 8088 registers. The prologue of each BIOS function indicates the registers used on the call and the return. For the memory size example above, no parameters are passed, and the result, memory size in 1K Byte increments is returned in the AX register.

Where a BIOS function has several possible operations, the AH register is used on input to indicate the desired operation. For example, to set the time of day, the following code is required.

```
MOV AH,1 ;function is to set time of
day.
MOV CX,HIGH_COUNT ;establish the current time.
MOV DX,LOW_COUNT
INT 1AH ;Set the time.

While to read the time of day:
MOV AH,0 ;function is to read the time
of day.
INT 1AH ;read the timer.
```

As a general rule, the BIOS routines preserve all registers except for AX and the flags. Other registers are modified on return only if they are returning a value to the caller. The exact register usage can be seen in the prologue of each BIOS function.

Interrupt Vector Listing

Interrupt Number	Name	BIOS Initialization
0	Divide by Zero	None
1	Single Step	None
2	Non Maskable	NMI_INT (F000:E2C3)
3	Breakpoint	None
4	Overflow	None
5	Print Screen	PRINT_SCREEN (F000:FF54)
6	Unused	
7	Unused	
8	Time of Day	TIMER_INT (F000:FEA5)
9	Keyboard	KB_INT (F000:E987)
A	Unused	
8259	Unused	
Interrupt	Unused (Reserved Communications)	
C	Unused	
D	Unused	
Vectors	Diskette	DISK_INT (F000:EF57)
E	Unused (Reserved Printer)	
F	Unused	
10	Video	VIDEO_INT (F000:F065)
11	Equipment Check	EQUIPMENT (F000:F84D)
12	Memory	MEMORY_SIZE_DETERMINE (F000:F841)
13	Diskette	DISKETTE_INT (F000:EC59)
14	Communications	RS232C_INT (F000:E739)
15	Cassette	CASSETTE_INT (F000:F859)
16	Entry	KEYBOARD_INT (F000:E82E)
17	Keyboard	PRINTER_INT (F000:EF02)
18	Printer	(F000:0000)
19	Cassette BASIC	BOOTSTRAP (F000:EF02)
1A	Bootstrap	TIME_OF_DAY (F000:FE6E)
1B	Time of Day	DUMMY_RETURN (F000:FF53)
18	Keyboard Break	DUMMY_RETURN (F000:FF53)
1C	Timer Tick	
1D	Video Initialization	VIDEO_PARAMS (F000:F044)
1E	Diskette Parameters	DISK_BASE (F000:EF07)
1F	Video Graphics Chars	None

Vectors with Special Meanings

Interrupt 1BH – Keyboard Break Address

This vector points to the code to be exercised when the CTRL BREAK keys are depressed on the keyboard. The vector is invoked while responding to the keyboard interrupt, and control should be returned via an IRET instruction. The power on routines initialize this vector to point to an IRET instruction, so that nothing happens when CTRL BREAK keys are depressed unless the application program sets a different value.

Control may be retained by this routine, with the following problems. The BREAK may have occurred during interrupt processing, so that one or more End of Interrupt commands must be set to the 8259 controller. Also, all I/O devices should be reset in case an operation was underway at that time.

Interrupt 1CH – Timer Tick

This vector points to the code to be executed on every tick of the system clock. This vector is invoked while responding to the timer interrupt, and control should be returned via an IRET instruction. The power on routines initialize this vector to point to an IRET instruction, so that nothing happens unless the application modifies the pointer. It is the responsibility of the application to save and restore all registers that will be modified.

Interrupt 1DH – Video Parameters

This vector points to a data region containing the parameters required for the initialization of the 6845 on the video card. Note that there are four separate tables, and all four must be reproduced if all modes of operation are to be supported. The power on routines initialize this vector to point to the parameters contained in the ROM video routine.

Interrupt 1EH – Diskette Parameters

This vector points to a data region containing the parameters required for the diskette drive. The power on routines initialize the vector to point to the parameters contained in the ROM diskette routine. These default parameters represent the specified values for any IBM drives attached to the machine. Changing this parameter block to reflect the specifications of the other drives attached may be necessary.

Interrupt 1FH – Graphics Character Extensions

When operating in the graphics modes of the Color/Graphics Monitor Adapter (320 x 200 or 640 x 200), the read/write character interface will form the character from the ASCII code point, using a set of dot patterns. The dot patterns for the first 128 code points are contained in ROM. To access the other 128 code points, this vector must be established to point at a table of up to 1K bytes, where each code point is represented by 8 bytes of graphic information. At power on this vector is initialized to 0:0, and it is the responsibility of the user to change this vector if the additional code points are required.

Other Read/Write Memory Usage

The IBM ROM BIOS routines use 256 bytes of memory starting at absolute 400 to 4FF. Locations 400-407 contain the base addresses of any RS232 cards attached to the system, 0's if none attached. These locations, in order, represent the 0 to 3 values used as the parameter to the RS232 BIOS routine. Locations 408-40F provide the same function, but for the PRINTER.

Memory locations 300-3FF are used as a stack area during the power on initialization, and the bootstrap, when control passed to it from power on. If the user desires the stack in a different area, it must be set by the application.

Note: Use the Interrupt Vector Listing as an aid to locate these topics in the ROM BIOS listing, Appendix "A".

BIOS Programming Tip

When programming with BIOS you should keep in mind that if an error is reported by the diskette code, to reset the diskette adapter and retry the operation. A specified number of retries should be required on reads to ensure the problem is not due to motor start-up.

BIOS Memory Map

STARTING ADDRESS HEX	
00000	BIOS INTERRUPT VECTORS
00080	AVAILABLE INTERRUPT VECTORS
00400	BIOS DATA AREA
00500	USER READ/ WRITE MEMORY
F4000	USER READ ONLY MEMORY
F6000	CASSETTE BASIC INTERPRETER
FE000	BIOS PROGRAM AREA

Figure 29. BIOS MEMORY MAP

BIOS Cassette Logic Software Algorithms

Interrupt 15

The cassette routine will be called with the request type in AH and the address of the bytes to be read or written will be specified by (ES):(BX) and the number of bytes to read/write will be specified by (CX). The actual number of bytes read will be returned in (DX). Read block and write block will automatically turn the motor on at the start and off at the end. The requests are as follows:

- (AH) = 0 Turn the cassette motor on.
- (AH) = 1 Turn the cassette motor off.
- (AH) = 2 (Read Block) Read (CX) bytes into memory beginning at address (ES):(BX) and return actual number of bytes read in (DX). Return the cassette status in (AH).
- (AH) = 3 (Write Block) Write (CX) bytes onto the cassette beginning at address (DS):(BX). Return the cassette status in (AH).

STATUS:

- AH = 00 No errors
- AH = 01 CRC-Error (Read Block)
- AH = 02 No data transitions
- AH = 04 No leader
- AH = 80 Invalid command

Note: The carry flag will be set on any error.

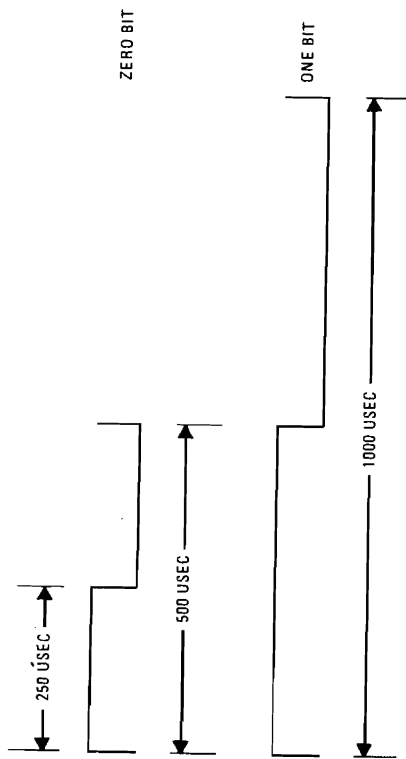
Cassette Write

The WRITE BLOCK routine writes a tape block on the cassette. The tape block is described in Data Record Architecture page (3-10).

The WRITE BLOCK routine turns on the cassette motor and a synchronization bit (0) and then writes 256 bytes of all ones, the leader, to the tape. Next, one or more data blocks are written (depends on number in CX). After each data block of 256 bytes, a two byte CRC is written. The data bytes are taken from the memory location pointed at by ES.

The WRITE BYTE routine disassembles the byte and writes it a bit at a time to the cassette. The method used is to set TIMER 2 to the period of the desired data bit. The timer is set to a period of 1.0 millisecond for a one bit and 0.5 millisecond for a zero bit.

The timer is set mode 3 which means it will output a square wave with period given by its count register. The timer's period is changed on the fly for each data bit to be written to the cassette. If the number of data bytes to be written is not an integral multiple of 256, then after the last desired data byte from memory has been written, the data block will be extended to 256 bytes by writing multiples of the last data byte. The last block will be closed with two CRC bytes as usual. After the last data block, a trailer consisting of four bytes of all one bits will be written. Finally, the motor will be turned off. There are no errors reported by this routine.



Cassette Read

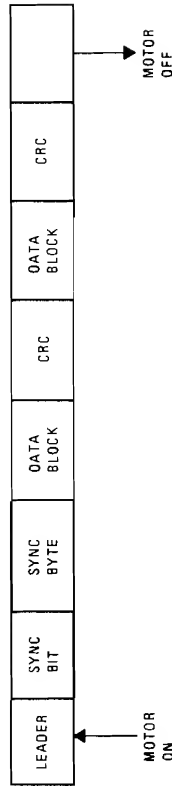
The READ BLOCK routine turns on the cassette motor and then delays for approximately 0.5 secs for it to come up to speed.

The READ BLOCK routine then searches for leader and must detect all one bits for approximately 1/4 of leader length before it can look for the sync byte. If a correct sync byte (X'16') is not found, the routine goes back and searches for leader again. The data is read a bit at a time and assembled into bytes. After each byte is assembled it is written into memory at location ES:BX and then BX is incremented by one.

After each multiple of 256 data bytes are read, the CRC is read and compared to the CRC generated. If a CRC error is detected, the routine will exit with the carry flag set to indicate an error and status (AH)-01 for CRC error. DX will contain the number of bytes written into memory.

Note: The Time of Day Interrupt (IRQ0) is disabled during the cassette read operation.

Data Record Architecture



1. Leader 256 bytes (of ones)
2. Sync byte ASCII Sync Char (X'16')
3. Sync byte (X'16')
4. Data Blocks 256 bytes
5. CRC — 2 bytes — for each data block

Error Recovery

Error recovery is handled by software. A cyclic redundancy check (CRC) is used to detect errors. The polynomial used is:

$$G(X) - X^{16} \ll X^{12} \ll X^5 \ll X^1$$

Which is the polynomial used by the SDLC interface. Essentially, as bits are written/read from tape, they are passed through the CRC-register in software. After a block of data is written, the complemented value of the calculated CRC-register is written on tape. On reading the cassette data, the CRC bytes are read and compared to the generated CRC value. If the read CRC does not equal the generated one, the processor's carry flag is set and status (AH) is set to X'01' to indicate a CRC error has occurred. Also, the routine is exited on CRC error.

Keyboard Encoding and Usage

Encoding

The keyboard routine provided by IBM in ROM BIOS is responsible for converting the keyboard scan codes into what will be termed "Extended ASCII".

Extended ASCII encompasses one byte character codes with possible values of 0-255, an extended code for certain extended keyboard functions and functions that are handled within the keyboard routine or through interrupts.

Character Codes

The following character codes are passed through the BIOS keyboard routine to the system or application program. A "[]" means the combination is suppressed in the keyboard routine. The codes are returned in AL. See Appendix C for exact codes. Use keyboard Scan Code diagram for reference page 2-23.

Table 25. Character Codes (U.S. Keyboard Layout)

KEY #	BASE CASE	UPPER CASE	CTRL	ALT
1	ESC	ESC	ESC	-1
2	1	1/2	-1	Note 1
3	2	@	NUL (000) Note 1	Note 1
4	3	#	-1	Note 1
5	4	\$	-1	Note 1
6	5	%	-1	Note 1
7	6	&	RS (030)	Note 1
8	7	*	-1	Note 1
9	8	+	-1	Note 1
10	9	(-1	Note 1
11	0)	-1	Note 1
12	-	-	US (031)	Note 1
13	=	+	-1	Note 1
14	Backspace (008)	Backspace (008)	DEL (127)	-1
15	→ (009)	← (Note 1)	-1	-1
16	q	Q	DC1 (017)	Note 1
17	w	W	ETB (023)	Note 1
18	e	E	ENQ (005)	Note 1
19	r	R	DC2 (018)	Note 1
20	t	T	DC4 (020)	Note 1
21	y	Y	EM (025)	Note 1
22	u	U	NAK (021)	Note 1
23	i	I	HT (009)	Note 1
24	o	O	SI (015)	Note 1
25	p	P	DLE (016)	Note 1
26	[{	ESC (027)	-1
27]	}	GS (029)	-1

Table 25. Character Codes (continued)

KEY #	BASE CASE	UPPER CASE	CTRL	ALT
28	CR	CR	LF (010)	-1
29	-1	-1	-1	-1
30	a	A	SOH (001)	Note 1
31	s	S	DC3 (019)	Note 1
32	d	D	EOT (004)	Note 1
33	f	F	ACK (006)	Note 1
34	g	G	BEL (007)	Note 1
35	h	H	BS (008)	Note 1
36	j	J	LF (010)	Note 1
37	k	K	VT (011)	Note 1
38	l	L	FF (012)	Note 1
39	;	;	-1	-1
40	,	,	-1	-1
41	'	'	-1	-1
42	-1	-1	-1	-1
43	\	-1	FS (028)	-1
44	z	Z	SUB (026)	Note 1
45	x	X	CAN (024)	Note 1
46	c	C	ETX (003)	Note 1
47	v	V	SYN (022)	Note 1
48	b	B	STX (002)	Note 1
49	n	N	SO (014)	Note 1
50	m	M	CR (013)	Note 1
51)	<	-1	-1
52	.	>	-1	-1
53	/	?	-1	-1
54	-1	-1	(Note 1)	-1
55	*	(Note 2)	-1	-1
56	-1	-1	-1	-1
57	SP	SP	SP	SP
58	-1	-1	-1	-1
59	NUL (Note 1)	NUL (Note 1)	NUL (Note 1)	NUL (Note 1)
60	NUL (Note 1)	NUL (Note 1)	NUL (Note 1)	NUL (Note 1)
61	NUL (Note 1)	NUL (Note 1)	NUL (Note 1)	NUL (Note 1)
62	NUL (Note 1)	NUL (Note 1)	NUL (Note 1)	NUL (Note 1)
63	NUL (Note 1)	NUL (Note 1)	NUL (Note 1)	NUL (Note 1)
64	NUL (Note 1)	NUL (Note 1)	NUL (Note 1)	NUL (Note 1)
65	NUL (Note 1)	NUL (Note 1)	NUL (Note 1)	NUL (Note 1)
66	NUL (Note 1)	NUL (Note 1)	NUL (Note 1)	NUL (Note 1)
67	NUL (Note 1)	NUL (Note 1)	NUL (Note 1)	NUL (Note 1)
68	NUL (Note 1)	NUL (Note 1)	NUL (Note 1)	NUL (Note 1)
69	-1	-1	Pause	-1
70	-1	-1	(Note 2)	-1
71	-1	-1	Break	-1
72	-1	-1	(Note 2)	-1

Note 1: Refer to Extended Codes Page (3-13).

Note 2: Refer to Special Handling Page (3-15).

Keys 71-83 have meaning only in base case, in NUMLOCK (or shifted) states, or in CTRL state. It should be noted that the shift key temporarily reverses the current NUMLOCK state.

KEY #	NUM LOCK	BASE CASE	ALT	CTRL
71	7	Home (Note 1)	Note 1	Clear Screen
72	8	↑ (Note 1)	Note 1	-1
73	9	PageUp (Note 1)	Note 1	Top of Text & Home
74	-	-	-1	-1
75	4	← (Note 1)	Note 1	Reverse Word (Note 1)
76	5	-1	Note 1	-1
77	6	→ (Note 1)	Note 1	Adv Word (Note 1)
78	+	+	-1	-1
79	1	End (Note 1)	Note 1	Erase to EOL (Note 1)
80	2	↓ (Note 1)	Note 1	-1
81	3	PageDown (Note 1)	Note 1	Erase to EOS (Note 1)
82	0	INS	Note 1	-1
83		DEL (Notes 1,2)	Note 2	Note 2

Note 1: Refer to Extended Codes Page (3-13).

Note 2: Refer to Special Handling Page (3-15).

Extended Codes

A. Extended Functions

For certain functions that cannot be represented in the standard ASCII code, an extended code is used. A character code of 000 (NUL) is returned in AL. This indicates that the system or application program should examine a second code that will indicate the actual function. Usually, but not always, this second code is the scan code of the primary key that was pressed. This code is returned in AH.

Table 26. Keyboard Extended Functions

SECOND CODE	FUNCTION
3	NUL Character
15	←
16-25	ALT Q, W, E, R, T, Y, U, I, O, P
30-38	ALT A, S, D, F, G, H, J, K, L
44-50	ALT Z, X, C, V, B, N, M
59-68	F1-F10 Function Keys Base Case
71	Home
72	↑
73	Page Up & Home Cursor
75	←
77	→
79	End
80	↓
81	Page Down & Home Cursor
82	INS
83	DEL
84-93	F11-F20 (Upper Case F1-F10)
94-103	F21-F30 (CTRL F1-F10)
104-113	F31-F40 (ALT F1-F10)
114	CTRL PRTSC (Start/Stop Echo to Printer) Key 55
115	CTRL ← Reverse Word
116	CTRL → Advance Word
117	CTRL END Erase EOL
118	CTRL PG DN Erase EOS
119	CTRL HOME Clear Screen and home
120-131	ALT 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, -, = (Keys 2-13)
132	CTRL PG UP TOP 25 Lines of Text & Home Cursor

ALT – Temporarily shifts keys 2-13, 16-25, 30-38, 44-50, and 59-68 to ALT state. Used with CTRL and DEL to cause system reset function described in Section I.3.

ALT has a special use to allow the user to enter any character code (0-255) into the system from the keyboard. The user holds down the ALT key and types the decimal value of characters using the numeric keyboard (keys 71-73, 75-77, 79-82). The ALT key is then released. If more than three digits are typed, a modulo 256 result is created. These three keys are interpreted as a character code (000-255) and are transmitted through the keyboard routine to the system or application program. ALT is handled internal to keyboard routine.

CAPS LOCK – Shifts keys 16-25, 30-38, 44-50 to upper case. A second depression of CAPS LOCK reverses the action. Handled internal to keyboard routine.

NUM LOCK – Shifts keys 71-73, 75-77, 79-83 to numeric state. A second depression of NUM LOCK reverses the action. Handled internal to keyboard routine.

SCROLL LOCK – Interpreted by appropriate application programs as indicating that the use of the cursor control keys should cause windowing over the text rather than cursor movement. A second depression of SCROLL LOCK reverses the action. The keyboard routine simply records the current shift state of SCROLL LOCK. It is up to the system or application program to perform the function.

C. Shift Key Priorities and Combinations

If combinations of ALT, CTRL and SHIFT are pressed and only one is valid, the precedence is as follows: Highest is ALT, then CTRL, then SHIFT. The only valid combination is ALT CTRL, which is used in system reset.

Special Handling

A. System Reset

The combination of ALT CTRL DEL (Key 83) will result in the keyboard routine initiating the equivalent of a system reset/reboot. Handled internal to keyboard routine.

B. Shift States

Most shift states are handled within the keyboard routine transparent to the system or application program. In any case, the current set of active shift states are available by calling an entry point in the ROM keyboard routine. The following keys result in altered shift states:

Shift – Temporarily shifts keys 2-13, 15-27, 30-41, 43-53, 55, 59-68 to upper case (lower case if in CAPSLOCK state). Temporarily reverses NUMLOCK/NUMLOCK state of keys 71-73, 75, 77, 79-83.

CTRL – Temporarily shifts keys 3, 7, 12, 14, 16-28, 30-38, 43-50, 55, 59-71, 73, 75, 77, 79, 81 to CTRL state. Used with ALT and DEL to cause "system reset" function described in Section I.3. Used with SCROLL LOCK to cause "break" function described in Section I.3. Used with NUMLOCK to cause "pause" function described in Section I.3.

B. Break

The combination CTRL BREAK will result in the keyboard routine signaling interrupt -1A. Also, the extended characters (AL = 00H, AH = 00H) will be returned.

Power up initialization, this interrupt is set up to cause the break sequence to be ignored. It is up to the system or application initialization code to change the interrupt vector in order to support an actual "break" function.

C. Pause

The combination CTRL NUM-LOCK will cause the keyboard interrupt routine to loop, waiting for any key except NUM-LOCK to be pressed. This provides a system/application transparent method of suspending list/print/etc. temporarily, and then resuming. The "Unpause" key is thrown away. Handled internal to keyboard routine.

The following keys will have their typematic action suppressed by the keyboard routine: CTRL, SHIFT, ALT, NUM-LOCK, SCROLL-LOCK, CAPS LOCK, INS.

E. Print Screen

The combination SHIFT-PRINT SCREEN (Key 55) will result in an interrupt invoking the print screen routine. This routine works in alpha/graphics mode, with unrecognizable characters printing as blanks.

The keyboard routine does its own buffering. The buffer is big enough to support a fast typist. If a key is entered when the buffer is full, the key will be ignored and the "bell" will be sounded.

Keyboard Usage

This section is intended to outline a set of guidelines for key usage when performing commonly used functions.

Table 27. Keyboard - Commonly Used Functions

FUNCTION	KEY(S)	COMMENT
Home Cursor	HOME	Editors; word processors
Return to outermost menu	HOME	Menu driven applications
Move cursor up	↑	Full screen editor, word processor
Page up, scroll backwards 25 lines & home	PG UP	Editors; word processors
Move cursor left	← Key 75	Text, command entry
Move cursor right	→	Text, command entry
Scroll to end of text Place cursor at end of line	END	Editors; word processors
Move cursor down	↓	Full screen editor, word processor
Page down, scroll forwards 25 lines & home	PG DN	Editors; word processors
Start/Stop insert text at cursor, shift text right in buffer	INS	Text, command entry
Delete character at cursor	DEL	Text, command entry
Destructive backspace	← Key 14	Text, command entry
Tab forward	→	Text entry
Tab reverse	←	Text entry
Clear screen and home	CTRL HOME	Command entry
Scroll up	↑	In scroll lock mode
Scroll down	↓	In scroll lock mode
Scroll left	←	In scroll lock mode
Scroll right	→	In scroll lock mode
Delete from cursor to EOL	CTRL END	Text, command entry
Exit/Escape	ESC	Editor, 1 level of menu, etc
Start/Stop Echo screen to printer	PRATSC CTRL K55	Any time
Delete from cursor to EOS	CTRL PG DN	Text, command entry

Table 27. Keyboard – Commonly Used Functions (continued)

FUNCTION	KEY(S)	COMMENT
Advance word	CTRL →	Text entry
Reverse word	CTRL ←	Text entry
Window Right	CTRL →	When text is too wide to fit screen
Window Left	CTRL ←	When text is too wide to fit screen
Enter insert mode	INS	Line editor
Exit insert mode	INS	Line editor
Cancel current line	ESC	Command entry, text entry
Suspend system (pause)	CTRL NUMLOCK	Stop list, stop program, etc. Resumes on any key
Break interrupt	CTRL BREAK	Interrupt current process
System reset	ALT CTRL DEL	Reboot
Top of document and home cursor	CTRL PG UP	Editors, word processors
Standard Function Keys	F1–F10	Primary function keys
Secondary function keys	SHIFT F1–F10 CTRL F1–F10 ALT F1–F10	Extra function keys if 10 are not sufficient
Extra function keys	ALT Keys 2–13 (1–9, 0, –, =)	Used when stickers are put along top of keyboard
Extra function keys	ALT A–Z	Used when function starts with same letter as one of the alpha keys

Table 28. BASIC Screen Editor Special Functions

FUNCTION	KEY
Carriage return	↵
Line feed	CTRL ↵
Bell	CTRL G
Home	HOME
Cursor up	↑
Cursor down	↓
Cursor left	←
Cursor right	→
Advance one word	CTRL →
Reverse one word	CTRL ←
Insert	INS
Delete	DEL
Clear screen	CTRL HOME
Freeze output	CTRL NUMLOCK
Tab advance	→
Stop execution (break)	CTRL BREAK
Delete current line	ESC
Delete to end of line	CTRL END
Position cursor to end of line	END

Table 29. DOS Special Functions

FUNCTION	KEY
Suspend	CTRL NUMLOCK
Echo to printer	CTRL-PRTS
Stop echo to printer	(Key 55 any case) CTRL-PRTS
Exit current function (break)	(Key 55 any case) CTRL BREAK
Backspace	← Key 14
Line feed	CTRL ↵
Cancel line	ESC
Copy character	F1 or →
Copy till match	F2
Copy remaining	F3
Skip character	DEL
Skip until match	F4
Enter insert mode	INS
Exit insert mode	INS
Make new line the template	F5
String separator in REPLACE	F6
End of file in keyboard input	F6

Low Memory Maps (0-0600'x)

ROM

Table 30. Interrupt Vectors (0-7F)

ADDRESS HEX	INTERRUPT HEX	FUNCTION
0-3	0	Divide by Zero
4-7	1	Single step
8-B	2	Non-Maskable Interrupt (NMI)
C-F	3	Break Point Instruction ('CC'x)
10-13	4	Overflow
14-17	5	Print Screen
18-1F	6,7	Reserved
20-23	8	Timer (18.2 per second)
24-27	9	Keyboard Interrupt
28-37	A,B,C,D	Reserved
38-3B	E	Diskette Interrupt
3C-3F	F	Reserved
40-43	10	Video I/O Call
44-47	11	Equipment Check Call
48-4B	12	Memory Check Call
4C-4F	13	Diskette I/O Call
50-53	14	RS232 I/O Call
54-57	15	Cassette I/O Call
58-5B	16	Keyboard I/O Call
5C-5F	17	Printer I/O Call
60-63	18	ROM Basic Entry Code
64-67	19	Boot Strap Loader
68-6B	1A	Time of Day Call
6C-6F	1B	Get Control on Keyboard Break: Note 1
70-73	1C	Get Control on timer interrupt: Note 1
74-77	1D	Pointer to video initialization table: Note 2
78-7B	1E	Pointer to diskette parameter table: Note 2
7C-7F	1F	Pointer to table (1KB) for graphics character Generator for ASCII 128-255. Defaults to 0:0
Notes: (1) Initialized at power up to point to an IRET instruction. (2) Initialized at power up to point to tables in ROM.		

Table 31. BASIC & DOS Reserved Interrupts (80-3FF)

ADDRESS HEX	INTERRUPT HEX	FUNCTION
80-83	20	DOS Program Terminate
84-87	21	DOS Function Call
88-8B	22	DOS Terminate Address
8C-8F	23	DOS CTRL-BRK Exit Address
90-93	24	DOS Fatal Error Vector
94-97	25	DOS Absolute Disk read
98-9B	26	DOS Absolute Disk write
9C-9F	27	DOS Terminate, Fix in Storage
A0-FF	28-3F	Reserved for DOS
100-1FF	40-7F	Not Used
200-217	80-85	Reserved By BASIC
218-3C3	86-F0	Used by BASIC Interpreter while BASIC is Running.
3C4-3FF	F1-FF	Not Used

Table 32. Reserved Memory Locations (400-5FF)

ADDRESS HEX	MODE	FUNCTION
400-48F	ROM BIOS	See BIOS Listing
490-4CF	DOS	Used by DOS Mode Command
4D0-4EF		Reserved
4F0-4FF		Reserved as Intra-Application Communication area for any application.
500-5FF		Reserved for DOS and BASIC
500	DOS	Print Screen status flag store. 0-Print screen not active or successful print screen operation. 1-Print screen in progress. 255-Error encountered during print screen operation.
504	DOS	Single drive mode status byte.
510-511	BASIC	BASIC's segment address store.
512-515	BASIC	Clock interrupt vector segment: offset store.
516-519	BASIC	Break key interrupt vector segment: offset store.
51A-51D	BASIC	Disk error interrupt vector segment: offset store.

BASIC Workspace Variables

If you do DEF SEG (Default workspace segment)

	OFFSET	LENGTH
Line number of current line being executed	X '2E'	2
Line number of last error	X '347'	2
Offset into segment of start of program text	X '30'	2
Offset into of start of variables (end of program text 1-1)	X '358'	2
Keyboard buffer contents if 0-no rharaacters in buffer if 1-characters in buffer if you POKE & H6A, 0 you flush any characters in buffer	X '6A'	1

Example:

100 Print PEEK (&H2E) + 256*PEEK (&H2F)

100 { L H X '64' X '00' }

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LOC OBJ	LINE	SOURCE	LOC OBJ	LINE	SOURCE
	1	*****BIOS FOR IBM PERSONAL COMPUTER*****		76	CTL_SHIFT EQU 04H ; CONTROL SHIFT KEY DEPRESSED
	2	;		77	LEFT_SHIFT EQU 02H ; LEFT SHIFT KEY DEPRESSED
	3	;		80	RIGHT_SHIFT EQU 01H ; RIGHT SHIFT KEY DEPRESSED
0000	4	PORT_A EQU 60H ; 1655 PORT A ADDR		82	KB_FLAG_1 DB ? ; SECOND BYTE OF KEYBOARD STATUS
0001	5	PORT_B EQU 61H ; 1655 PORT B ADDR		83	INS_SHIFT EQU 00H ; INSERT KEY IS DEPRESSED
0002	6	PORT_C EQU 62H ; 1655 PORT C ADDR		84	CAPS_LOCK EQU 40H ; CAPS LOCK KEY IS DEPRESSED
0003	7	CPD_PORT EQU 63H ; 1655 PORT C ADDR		85	NUM_SHIFT EQU 20H ; NUM LOCK KEY IS DEPRESSED
0004	8	INTA0 EQU 20H ; 1655 PORT		86	SCROLL_SHIFT EQU 10H ; SCROLL LOCK KEY IS DEPRESSED
0005	9	INTA1 EQU 21H ; 1655 PORT		87	SCROLL_LOCK EQU 00H ; SCROLL LOCK HAS BEEN TOGGLED
0006	10	INTA2 EQU 22H ; 1655 PORT		88	ALT_INPUT DB ? ; STORAGE FOR ALTERNATE KEYPAD ENTRY
0007	11	INTA3 EQU 23H ; 1655 PORT		89	ALT_BUFFER EQU 00H ; POINTER TO HEAD OF KEYBOARD BUFFER
0008	12	INTA4 EQU 24H ; 1655 PORT		90	ALT_BUFFER_TAIL DB ? ; POINTER TO TAIL OF KEYBOARD BUFFER
0009	13	INTA5 EQU 25H ; 1655 PORT		91	KB_BUFFER EQU 16 DUP(?) ; ROOM FOR 16 ENTRIES
0010	14	INTA6 EQU 26H ; 1655 PORT		92	KB_BUFFER_END LABEL WORD
0011	15	INTA7 EQU 27H ; 1655 PORT		93	;
0012	16	INTA8 EQU 28H ; 1655 PORT		94	;
0013	17	INTA9 EQU 29H ; 1655 PORT		95	;
0014	18	INTA10 EQU 30H ; 1655 PORT		96	;
0015	19	INTA11 EQU 31H ; 1655 PORT		97	;
0016	20	INTA12 EQU 32H ; 1655 PORT		98	;
0017	21	INTA13 EQU 33H ; 1655 PORT		99	;
0018	22	INTA14 EQU 34H ; 1655 PORT		100	;
0019	23	INTA15 EQU 35H ; 1655 PORT		101	;
0020	24	INTA16 EQU 36H ; 1655 PORT		102	;
0021	25	INTA17 EQU 37H ; 1655 PORT		103	;
0022	26	INTA18 EQU 38H ; 1655 PORT		104	;
0023	27	INTA19 EQU 39H ; 1655 PORT		105	;
0024	28	INTA20 EQU 40H ; 1655 PORT		106	;
0025	29	INTA21 EQU 41H ; 1655 PORT		107	;
0026	30	INTA22 EQU 42H ; 1655 PORT		108	;
0027	31	INTA23 EQU 43H ; 1655 PORT		109	;
0028	32	INTA24 EQU 44H ; 1655 PORT		110	;
0029	33	INTA25 EQU 45H ; 1655 PORT		111	;
0030	34	INTA26 EQU 46H ; 1655 PORT		112	;
0031	35	INTA27 EQU 47H ; 1655 PORT		113	;
0032	36	INTA28 EQU 48H ; 1655 PORT		114	;
0033	37	INTA29 EQU 49H ; 1655 PORT		115	;
0034	38	INTA30 EQU 50H ; 1655 PORT		116	;
0035	39	INTA31 EQU 51H ; 1655 PORT		117	;
0036	40	INTA32 EQU 52H ; 1655 PORT		118	;
0037	41	INTA33 EQU 53H ; 1655 PORT		119	;
0038	42	INTA34 EQU 54H ; 1655 PORT		120	;
0039	43	INTA35 EQU 55H ; 1655 PORT		121	;
0040	44	INTA36 EQU 56H ; 1655 PORT		122	;
0041	45	INTA37 EQU 57H ; 1655 PORT		123	;
0042	46	INTA38 EQU 58H ; 1655 PORT		124	;
0043	47	INTA39 EQU 59H ; 1655 PORT		125	;
0044	48	INTA40 EQU 60H ; 1655 PORT		126	;
0045	49	INTA41 EQU 61H ; 1655 PORT		127	;
0046	50	INTA42 EQU 62H ; 1655 PORT		128	;
0047	51	INTA43 EQU 63H ; 1655 PORT		129	;
0048	52	INTA44 EQU 64H ; 1655 PORT		130	;
0049	53	INTA45 EQU 65H ; 1655 PORT		131	;
0050	54	INTA46 EQU 66H ; 1655 PORT		132	;
0051	55	INTA47 EQU 67H ; 1655 PORT		133	;
0052	56	INTA48 EQU 68H ; 1655 PORT		134	;
0053	57	INTA49 EQU 69H ; 1655 PORT		135	;
0054	58	INTA50 EQU 70H ; 1655 PORT		136	;
0055	59	INTA51 EQU 71H ; 1655 PORT		137	;
0056	60	INTA52 EQU 72H ; 1655 PORT		138	;
0057	61	INTA53 EQU 73H ; 1655 PORT		139	;
0058	62	INTA54 EQU 74H ; 1655 PORT		140	;
0059	63	INTA55 EQU 75H ; 1655 PORT		141	;
0060	64	INTA56 EQU 76H ; 1655 PORT		142	;
0061	65	INTA57 EQU 77H ; 1655 PORT		143	;
0062	66	INTA58 EQU 78H ; 1655 PORT		144	;
0063	67	INTA59 EQU 79H ; 1655 PORT		145	;
0064	68	INTA60 EQU 80H ; 1655 PORT		146	;
0065	69	INTA61 EQU 81H ; 1655 PORT		147	;
0066	70	INTA62 EQU 82H ; 1655 PORT		148	;
0067	71	INTA63 EQU 83H ; 1655 PORT		149	;
0068	72	INTA64 EQU 84H ; 1655 PORT		150	;
0069	73	INTA65 EQU 85H ; 1655 PORT		151	;
0070	74	INTA66 EQU 86H ; 1655 PORT		152	;
0071	75	INTA67 EQU 87H ; 1655 PORT		153	;
0072	76	INTA68 EQU 88H ; 1655 PORT		154	;
0073	77	INTA69 EQU 89H ; 1655 PORT		155	;
0074	78	INTA70 EQU 90H ; 1655 PORT		156	;
0075	79	INTA71 EQU 91H ; 1655 PORT		157	;
0076	80	INTA72 EQU 92H ; 1655 PORT		158	;
0077	81	INTA73 EQU 93H ; 1655 PORT		159	;
0078	82	INTA74 EQU 94H ; 1655 PORT		160	;
0079	83	INTA75 EQU 95H ; 1655 PORT		161	;
0080	84	INTA76 EQU 96H ; 1655 PORT		162	;
0081	85	INTA77 EQU 97H ; 1655 PORT		163	;
0082	86	INTA78 EQU 98H ; 1655 PORT		164	;
0083	87	INTA79 EQU 99H ; 1655 PORT		165	;
0084	88	INTA80 EQU 100H ; 1655 PORT		166	;
0085	89	INTA81 EQU 101H ; 1655 PORT		167	;
0086	90	INTA82 EQU 102H ; 1655 PORT		168	;
0087	91	INTA83 EQU 103H ; 1655 PORT		169	;
0088	92	INTA84 EQU 104H ; 1655 PORT		170	;
0089	93	INTA85 EQU 105H ; 1655 PORT		171	;
0090	94	INTA86 EQU 106H ; 1655 PORT		172	;
0091	95	INTA87 EQU 107H ; 1655 PORT		173	;
0092	96	INTA88 EQU 108H ; 1655 PORT		174	;
0093	97	INTA89 EQU 109H ; 1655 PORT		175	;
0094	98	INTA90 EQU 110H ; 1655 PORT		176	;
0095	99	INTA91 EQU 111H ; 1655 PORT		177	;
0096	100	INTA92 EQU 112H ; 1655 PORT		178	;
0097	101	INTA93 EQU 113H ; 1655 PORT		179	;
0098	102	INTA94 EQU 114H ; 1655 PORT		180	;
0099	103	INTA95 EQU 115H ; 1655 PORT		181	;
0100	104	INTA96 EQU 116H ; 1655 PORT		182	;
0101	105	INTA97 EQU 117H ; 1655 PORT		183	;
0102	106	INTA98 EQU 118H ; 1655 PORT		184	;
0103	107	INTA99 EQU 119H ; 1655 PORT		185	;
0104	108	INTA100 EQU 120H ; 1655 PORT		186	;
0105	109	INTA101 EQU 121H ; 1655 PORT		187	;
0106	110	INTA102 EQU 122H ; 1655 PORT		188	;
0107	111	INTA103 EQU 123H ; 1655 PORT		189	;
0108	112	INTA104 EQU 124H ; 1655 PORT		190	;
0109	113	INTA105 EQU 125H ; 1655 PORT		191	;
0110	114	INTA106 EQU 126H ; 1655 PORT		192	;
0111	115	INTA107 EQU 127H ; 1655 PORT		193	;
0112	116	INTA108 EQU 128H ; 1655 PORT		194	;
0113	117	INTA109 EQU 129H ; 1655 PORT		195	;
0114	118	INTA110 EQU 130H ; 1655 PORT		196	;
0115	119	INTA111 EQU 131H ; 1655 PORT		197	;
0116	120	INTA112 EQU 132H ; 1655 PORT		198	;
0117	121	INTA113 EQU 133H ; 1655 PORT		199	;
0118	122	INTA114 EQU 134H ; 1655 PORT		200	;
0119	123	INTA115 EQU 135H ; 1655 PORT		201	;
0120	124	INTA116 EQU 136H ; 1655 PORT		202	;
0121	125	INTA117 EQU 137H ; 1655 PORT		203	;
0122	126	INTA118 EQU 138H ; 1655 PORT		204	;
0123	127	INTA119 EQU 139H ; 1655 PORT		205	;
0124	128	INTA120 EQU 140H ; 1655 PORT		206	;
0125	129	INTA121 EQU 141H ; 1655 PORT		207	;
0126	130	INTA122 EQU 142H ; 1655 PORT		208	;
0127	131	INTA123 EQU 143H ; 1655 PORT		209	;
0128	132	INTA124 EQU 144H ; 1655 PORT		210	;
0129	133	INTA125 EQU 145H ; 1655 PORT		211	;
0130	134	INTA126 EQU 146H ; 1655 PORT		212	;
0131	135	INTA127 EQU 147H ; 1655 PORT		213	;
0132	136	INTA128 EQU 148H ; 1655 PORT		214	;
0133	137	INTA129 EQU 149H ; 1655 PORT		215	;
0134	138	INTA130 EQU 150H ; 1655 PORT		216	;
0135	139	INTA131 EQU 151H ; 1655 PORT		217	;
0136	140	INTA132 EQU 152H ; 1655 PORT		218	;
0137	141	INTA133 EQU 153H ; 1655 PORT		219	;
0138	142	INTA134 EQU 154H ; 1655 PORT		220	;
0139	143	INTA135 EQU 155H ; 1655 PORT		221	;
0140	144	INTA136 EQU 156H ; 1655 PORT		222	;
0141	145	INTA137 EQU 157H ; 1655 PORT		223	;
0142	146	INTA138 EQU 158H ; 1655 PORT		224	;
0143	147	INTA139 EQU 159H ; 1655 PORT		225	;
0144	148	INTA140 EQU 160H ; 1655 PORT		226	;
0145	149	INTA141 EQU 161H ; 1655 PORT		227	;
0146	150	INTA142 EQU 162H ; 1655 PORT		228	;
0147	151	INTA143 EQU 163H ; 1655 PORT		229	;
0148	152	INTA144 EQU 164H ; 1655 PORT		230	;
0149	153	INTA145 EQU 165H ; 1655 PORT		231	;
0150	154	INTA146 EQU 166H ; 1655 PORT		232	;
0151	155	INTA147 EQU 167H ; 1655 PORT		233	;
0152	156	INTA148 EQU 168H ; 1655 PORT		234	;
0153	157	INTA149 EQU 169H ; 1655 PORT		235	;
0154	158	INTA150 EQU 170H ; 1655 PORT		236	;
0155	159	INTA151 EQU 171H ; 1655 PORT		237	;
0156	160	INTA152 EQU 172H ; 1655 PORT		238	;
0157	161	INTA153 EQU 173H ; 1655 PORT		239	;
0158	162	INTA154 EQU 174H ; 1655 PORT		240	;
0159	163	INTA155 EQU 175H ; 1655 PORT		241	;
0160	164	INTA156 EQU 176H ; 1655 PORT		242	;
0161	165	INTA157 EQU 177H ; 1655 PORT		243	;
0162	166	INTA158 EQU 178H ; 1655 PORT		244	;
0163	167	INTA159 EQU 179H ; 1655 PORT		245	;
0164	168	INTA160 EQU 180H ; 1655 PORT		246	;
0165	169	INTA161 EQU 181H ; 1655 PORT		247	;
0166	170	INTA162 EQU 182H ; 1655 PORT		248	;
0167	171	INTA163 EQU 183H ; 1655 PORT		249	;
0168	172	INTA164 EQU 184H ; 1655 PORT		250	;
0169	173	INTA165 EQU 185H ; 1655 PORT		251	;
0170	174	INTA166 EQU 186H ; 1655 PORT		252	;
0171	175	INTA167 EQU 187H ; 1655 PORT		253	;
0172	176	INTA168 EQU 188H ; 1655 PORT		254	;
0173	177	INTA169 EQU 189H ; 1655 PORT		255	;
0174	178	INTA170 EQU 190H ; 1655 PORT		256	;
0175	179	INTA171 EQU 191H ; 1655 PORT		257	;
0176	180	INTA172 EQU 192H ; 1655 PORT		258	;
0177	181	INTA173 EQU 193H ; 1655 PORT		259	;
0178	182	INTA174 EQU 194H ; 1655 PORT		260	;
0179	183	INTA175 EQU 195H ; 1655 PORT		261	;
0180	184	INTA176 EQU 196H ; 1655 PORT		262	;
0181	185	INTA177 EQU 197H ; 1655 PORT		263	;
0182	186	INTA178 EQU 198H ; 1655 PORT		264	;
0183	187	INTA179 EQU 199H ; 1655 PORT		265	;
0184	188	INTA180 EQU 200H ; 1655 PORT		266	;
0185	189	INTA181 EQU 201H ; 1655 PORT		267	;
0186	190	INTA182 EQU 202H ; 1655 PORT		268	;
0187	191	INTA183 EQU 203H ; 1655 PORT		269	;
0188	192	INTA184 EQU 204H ; 1655 PORT		270	;
0189	193	INTA185 EQU 205H ; 1655 PORT		271	;
0190	194	INTA186 EQU 206H ; 1655 PORT		272	;
0191	195	INTA187 EQU 207H ; 1655 PORT		273	;
0192	196	INTA188 EQU 208H ; 1655 PORT		274	;
0193	197	INTA189 EQU 209H ; 1655 PORT		275	;
0194	198	INTA190			

LOC OBJ	LINE	SOURCE	LOC OBJ	LINE	SOURCE
0068 ??	155	LAST_VAL DB ? ; LAST INPUT VALUE	E02A	229	DEC C3;
	156	;	E024 4F	230	DEC D1
	157	;	E020 F0	231	MOV SI,01
	158	;	E02C 88F7	232	MOV CX,BX
006C 7777	159	;	E028 AC	233	MOV LOD58
006E 7777	160	TIMER_LOW DB ? ; LOW WORD OF TIMER COUNT	E030 AC	234	XOR AL,AH
0070 ??	161	TIMER_HIGH DB ? ; HIGH WORD OF TIMER COUNT	E031 32C4	235	JNE C7
	162	TIMER_OFL DB ? ; TIMER HAS ROLLED OVER SINCE LAST READ	E035 7525	236	IN AL,PORT_C
	163	COUNTS_SEC EDI 18	E035 E442	237	AND AL,000H
	164	COUNTS_MIN EDI 1092	E037 24C0	238	MOV AL,0
	165	COUNTS_HOUR EDI 65543	E039 8000	239	JNZ C7
	166	COUNTS_DAY EDI 1573040 = 180080H	E03B 7510	240	JNZ C7
	167	;	E03D 00F000	241	CPH AH,0
	168	;	E040 76B3	242	JE C6
	169	;	E046 84C3	243	MOV AL,DL
0071 ??	170	;	E04A AA	244	STOSB
0072 7777	171	BIOS_BREAK DB ? ; BIT 7 = 1 IF BREAK KEY HAS BEEN DEPRESSED	E045 E2E9	245	LOOP CS;
	172	RESET_FLAG DB ? ; WORD = 1234H IF KEYBOARD RESET UNDERWAY	E047 60FC08	246	CHP C7
	173	DATA ENDS	E044 740E	247	JE C7
	174	;	E04C 84E0	248	MOV AH,AL
	175	;	E04E 88F2	249	XCHG DH,DL
	176	;	E050 FC	250	CLO
0050	177	;	E051 47	251	INC DI
0000 ??	178	XDATA SEGMENT AT 50H	E051 47	252	JZ C4
	179	STATUS_BYTE DB ?	E052 7408	253	DEC DI
	180	XDATA ENDS	E054 4F	254	DEC DI
	181	;	E055 8A0100	255	MOV DX,1
	182	;	E056 E800	256	JMP SHORT C3
	183	;	E05A	257	
	184	;	E05A C3	258	RET
0000	185	VIDEO_RAM SEGMENT AT 0800H	STATST ENDP	259	
0000	186	REGEND LABEL BYTE	TEST_01	260	
0000	187	REGEND LABEL WORD	DESCRIPTION	261	
0000 (16384 ??)	188	VIDEO_RAM DB 16384 DUP(?)	VERIFY 0008 FLAGS, REGISTERS AND CONDITIONAL JUMPS	262	
	189	VIDEO_RAM ENDS		263	
	190	;		264	
	191	;		265	
	192	;		266	
0000	193	CODE SEGMENT AT 0F00H	DISASSEMBLY INTERRUPTS	267	
0000 (57344 ??)	194	DB 57344 DUP(?) ; FILL LOWEST 56K	SET SF, CF, ZF, AND AF FLAGS ON	268	
	195	;		269	
0000 (57344 ??)	196	DB 57000511 COMP. IBM 1981 ; COPYRIGHT NOTICE		270	
	197	;		271	
0000 3573030303531	198	;		272	
0000 3573030303531	199	;		273	
0000 3573030303531	200	;		274	
0000 3573030303531	201	;		275	
0000 3573030303531	202	;		276	
0000 3573030303531	203	;		277	
0000 3573030303531	204	;		278	
0000 3573030303531	205	;		279	
0000 3573030303531	206	;		280	
0000 3573030303531	207	;		281	
0000 3573030303531	208	;		282	
0000 3573030303531	209	;		283	
0000 3573030303531	210	;		284	
0000 3573030303531	211	;		285	
0000 3573030303531	212	;		286	
0000 3573030303531	213	;		287	
0000 3573030303531	214	;		288	
0000 3573030303531	215	;		289	
0000 3573030303531	216	;		290	
0000 3573030303531	217	;		291	
0000 3573030303531	218	;		292	
0000 3573030303531	219	;		293	
0000 3573030303531	220	;		294	
0000 3573030303531	221	;		295	
0000 3573030303531	222	;		296	
0000 3573030303531	223	;		297	
0000 3573030303531	224	;		298	
0000 3573030303531	225	;		299	
0000 3573030303531	226	;		300	
0000 3573030303531	227	;		301	
0000 3573030303531	228	;		302	
0000 3573030303531	229	;		303	
0000 3573030303531	230	;		304	
0000 3573030303531	231	;		305	
0000 3573030303531	232	;		306	

LOC OBJ	LINE	SOURCE
E09E 88F5	307	MOV SI,BP
E0A0 88FE	308	MOV DI,SI
E0A2 7307	309	JNC C9
E0A4 33C7	310	XOP AX,DI
E0A6 7507	311	JNZ E8B0
E0A8 F8	312	CLC
E0A9 73E3	313	JNC C8
E0AB	314	C9:
E0AC 08C7	315	OP AX,DI
E0AD 7401	316	JZ C10
E0AF F4	317	ERR01: JLT
	318	-----
	319	:TEST 02
	320	: ROS CHECKSUM TEST 1
	321	: DESCRIPTION:
	322	: A CHECKSUM IS DONE FOR THE OK ROS MODULE CONTAINING P00 AND BIOS.
	323	-----
	324	C10:
E0B0 8000	325	MOV AL,0
E0B2 6640	326	OUT 0A0H,AL
E0B4 6643	327	OUT 0B1H,AL
E0B6 8099	328	MOV AL,7FH
E0B8 6643	329	OUT 0C0,PORT,AL
E0BA 807C	330	MOV AL,0FCH
E0BC 6641	331	OUT 0D0,PORT,AL
E0BE 74C0	332	SUB AL,AL
E0C0 8A0903	333	MOV DX,30BH
E0C2 EE	334	OUT DX,AL
E0C4 F6C0	335	INC AL
E0C6 C4B03	336	MOV DX,30BH
E0C8 EE	337	CUT DX,AL
E0CA 8A09F0	338	MOV AX,CODE
E0CC 8E00	339	MOV \$5,AX
E0CE B0D0E0	340	MOV DX,0E00H
E0D0 B0C4E0	341	MOV SP,OFFSET C1
E0D2 F93010	342	JMP POS CHECKSUM
E0D4 75D5	343	C11: JUE ERR01
	344	-----
	345	:TEST 03
	346	: 8332 DMA INITIALIZATION CHANNEL REGISTER TEST
	347	: DESCRIPTION:
	348	: DISABLE THE 8332 DMA CONTROLLER. VERIFY THAT TIMER 1 FUNCTIONS OK.
	349	: WRITE/READ THE CURRENT ADDRESS AND WORD COUNT REGISTERS FOR ALL
	350	: CHANNELS. INITIALIZE AND START DMA FOR MEMORY REFRESH.
	351	-----
	352	: DISABLE DMA CONTROLLER
E0E0 8004	353	MOV AL,04
E0E2 E608	354	OUT 0A00,AL
	355	-----
	356	: VERIFY THAT TIMER 1 FUNCTIONS OK
	357	-----
E0E6 8054	358	MOV AL,\$4H
E0E8 E643	359	OUT TIMER+3,AL
E0EA 20C9	360	SUB CX,CX
E0EC 9A09	361	MOV BL,CL
E0EE BAC1	362	MOV AL,CL
E0F0 E641	363	OUT TIMER+1,AL
E0F2 8040	364	MOV AL,\$0H
E0F4 B040	365	OUT TIMER+1,AL
E0F6 E643	366	IN AL,TIMER+1
E0F8 E641	367	OUT BL,AL
E0FA 0A0B	368	CMP BL,OFFH
E0FC 0070FF	369	JC C13
E0FE 7404	370	JE C13
E0FF E2F1	371	LOOP C12
E0FF E8B4	372	JMP SHORT ERR01
E0FF	373	-----
E0FF 8AC3	374	MOV AL,\$L
E0FF 20C9	375	SUB CX,CX
E0FF E641	376	OUT TIMER+1,AL
E101	377	OUT
E101 8040	378	MOV AL,\$0H
E103 E643	379	OUT TIMER+3,AL
E105 E641	380	IN AL,TIMER+1
E107 2208	381	MOV AL,AL
E109 7404	382	JZ C15
E10B E2F4	383	LOOP C14
	384	-----
	385	LOC OBJ
	386	E100 E840
	387	-----
	388	:TEST 04
	389	: BASE 16K READ/WRITE STORAGE TEST
	390	: DESCRIPTION:
	391	: WRITE/READ/VERIFY DATA PATTERNS FF,55,AA,01, AND 00 TO 1ST 16K OF
	392	: STORAGE. VERIFY STORAGE ADDRESSABILITY.
	393	: INITIALIZE THE 8350 INTERRUPT CONTROLLER CHIP FOR CHECKING
	394	: MANUFACTURING TEST 2 MODE.
	395	-----
	396	: DETERMINE REPORT SIZE AND FILL MEMORY WITH DATA
	397	-----
	398	MOV AX,DATA
	399	MOV DS,AX
	400	MOV BX,RESET_FLAG
	401	SUB BX,AX
	402	MOV ES,AX
	403	MOV DS,AX
	404	MOV DI,\$1
	405	SUB DI,DI
	406	MOV AL,\$0H
	407	OUT AL,PORT_A
	408	MOV AL,\$0H
	409	OUT AL,PORT_A
	410	ADD AL,4
	411	MOV CL,12
	412	SHL AX,CL
	413	MOV CX,AX
	414	MOV AH,AL
	415	CLO
	416	STOSB
	417	-----
	418	: INITIALIZE AND START DMA FOR MEMORY REFRESH.
	419	-----
	420	MOV AL,OFFH
	421	OUT 0A00,AL
	422	OUT 0A01,AL
	423	MOV AL,\$0BH
	424	OUT 0A00,AL
	425	MOV AL,0
	426	OUT 0A00,AL
	427	OUT 0A01,AL
	428	MOV AL,\$1H
	429	OUT 0A00,AL
	430	MOV AL,\$2H
	431	OUT 0A00,AL
	432	MOV AL,\$3H
	433	OUT 0A00,AL
	434	-----
	435	:TEST 04
	436	-----
	437	: WRITE/READ/VERIFY DATA PATTERNS FF,55,AA,01, AND 00 TO 1ST 16K OF
	438	: STORAGE. VERIFY STORAGE ADDRESSABILITY.
	439	: INITIALIZE THE 8350 INTERRUPT CONTROLLER CHIP FOR CHECKING
	440	: MANUFACTURING TEST 2 MODE.
	441	-----
	442	: DETERMINE REPORT SIZE AND FILL MEMORY WITH DATA
	443	-----
	444	MOV AX,DATA
	445	MOV DS,AX
	446	MOV BX,RESET_FLAG
	447	SUB BX,AX
	448	MOV ES,AX
	449	MOV DS,AX
	450	MOV DI,\$1
	451	SUB DI,DI
	452	MOV AL,\$0H
	453	OUT AL,PORT_A
	454	MOV AL,\$0H
	455	OUT AL,PORT_A
	456	ADD AL,4
	457	MOV CL,12
	458	SHL AX,CL
	459	MOV CX,AX
	460	MOV AH,AL
	461	CLO
	462	STOSB
	463	-----
	464	: INITIALIZE AND START DMA FOR MEMORY REFRESH.
	465	-----
	466	MOV AL,OFFH
	467	OUT 0A00,AL
	468	OUT 0A01,AL
	469	MOV AL,\$0BH
	470	OUT 0A00,AL
	471	MOV AL,0
	472	OUT 0A00,AL
	473	OUT 0A01,AL
	474	MOV AL,\$1H
	475	OUT 0A00,AL
	476	MOV AL,\$2H
	477	OUT 0A00,AL
	478	MOV AL,\$3H
	479	OUT 0A00,AL
	480	-----
	481	:TEST 04
	482	-----
	483	: WRITE/READ/VERIFY DATA PATTERNS FF,55,AA,01, AND 00 TO 1ST 16K OF
	484	: STORAGE. VERIFY STORAGE ADDRESSABILITY.
	485	: INITIALIZE THE 8350 INTERRUPT CONTROLLER CHIP FOR CHECKING
	486	: MANUFACTURING TEST 2 MODE.
	487	-----
	488	: DETERMINE REPORT SIZE AND FILL MEMORY WITH DATA
	489	-----
	490	MOV AX,DATA
	491	MOV DS,AX
	492	MOV BX,RESET_FLAG
	493	SUB BX,AX
	494	MOV ES,AX
	495	MOV DS,AX
	496	MOV DI,\$1
	497	SUB DI,DI
	498	MOV AL,\$0H
	499	OUT AL,PORT_A
	500	MOV AL,\$0H
	501	OUT AL,PORT_A
	502	ADD AL,4
	503	MOV CL,12
	504	SHL AX,CL
	505	MOV CX,AX
	506	MOV AH,AL
	507	CLO
	508	STOSB

LOC OBJ	LINE	SOURCE	LOC OBJ	LINE	SOURCE
E179 E2FD	462	LOOP C19	E1FA 2AC706B00C3E5 R	537	MOV ES:INT_PTR,OFFSET INT1_INT
	463		E201 2AC706B0A000F0 R	538	MOV ES:INT_PTR+2,CODE
	464		E208 E92A00	539	JMP TS10
	465			540	ROS_CHECKSUM
E17B E462	466	MOV AL,PORT_C	E20B 800E20	541	MOV CX,DIY2
E17D 2A0F	467	AND AL,0FH	E20C 32C0	542	XOR AL,AL
E17F 7A18	468	JZ C21	E210	543	C26:
E181 B40010	469	MOV DX,1000H	E210 2E0207	544	ADD AL,C5:10X1
E184 8A00	470	MOV AH,AL	E213 43	545	INC BX
E186 8000	471	MOV AL,0	E214 E2FA	546	LOOP C26
E188 0E0C	472	C20:	E216 0A00	548	OR AL,AL
E18A 850000	473	MOV ES,0X	E218 C3	549	BET
E18C 20FF	474	MOV CX,8000H	ROS_CHECKSUM	550	ENDP
E190 20FF	475	SUB DI,DI	-----	551	-----
E19F F3	476	REP STOSB	-----	552	-----
E190 AA	477	ADD DX,8000H	-----	553	-----
E191 01C20000	478	DEC AH	-----	554	-----
E195 FECC	479	JNZ C20	-----	555	-----
E197 75EF	480		-----	556	-----
	481	INITIALIZE THE 8259 INTERRUPT CONTROLLER CHIP	E219 50415249545920	557	D1 DB 'PARITY CHECK 2'
	482		43464543482032	558	D1L EQU 1-01
	483	C21:	000E	559	D2 DB 'PARITY CHECK 1'
E199 8013	484	MOV AL,13H	43464543482031	560	D2L EQU 1-02
E19B E620	485	OUT INTA00,AL	000E	561	TEST 06
E19D 8008	486	MOV AL,8		562	8259 INTERRUPT CONTROLLER TEST
E19F E621	487	OUT INTA01,AL		563	DESCRIPTION
E1A1 8009	488	MOV AL,9		564	POINT DS AND ES TO BEGIN
E1A3 E621	489	OUT INTA01,AL		565	OF RAM STORAGE
E1A5 28C0	490	SUB AX,AX		566	POINT DS TO DATA SEG
E1A7 80C0	491	MOV ES,AX		567	RESTORE RESET_FLAG
E1A9 BE4000	492	MOV SI,DATA		568	RESET_FLAG SET?
E1AC 80C0	493	MOV DS,SI		569	YES - SKIP STG TEST
E1AE 871E7200	494	MOV RESET_FLAG,BX		570	POINT DS TO 1ST 16K OF STG
E1B0 01C7200412	495	MOV RESET_FLAG,1234H		571	TEST PROGRAMS FROM KEYBOARD.
E1B2 7438	496	JE C25		572	-----
E1B4 8008	497	MOV DS,AX		573	-----
	498	CHECK FOR MANUFACTURING TEST 2 TO LOAD	E219 2AC706B14005A7F R	574	MOV ES:INTS_PTR,OFFSET PRINT_SCREEN
	499	-----	E240 2AC706B16000F0 R	575	MOV ES:INTS_PTR+2,CODE
	500	-----		576	TEST THE INT REGISTER
E1B8 B0F03F	501	MOV SP,3FFFH		577	CLI
E1BF 80C0	502	MOV SS,AX		578	DIABLE INTERRUPTS
E1C1 00F0	503	MOV DI,AX		579	SET INT TO ZERO
E1C3 B82400	504	MOV BX,24H		580	MOV AL,0
E1C6 C707B642	505	MOV WORD PTR [BX],OFFSET D11		581	OUT INTA01,AL
E1C8 43	506	INC BX		582	IN AL,INTA01
E1CB 43	507	INC BX		583	OR AL,AL
E1CC 80C0	508	MOV [BX],CS		584	JNZ D6
E1CE E8B794	509	CALL KBD RESET		585	MOV AL,0FH
E1D1 80F6A5	510	MOV BL,0A5H		586	OUT INTA01,AL
E1D4 750E	511	JNZ C23		587	IN AL,INTA01
E1D6 B2FF	512	CALL SP,TEST		588	ADD AL,1
E1D8 F8A0A4	513	MOV SP,TEST		589	JNZ D6
E1DA 8A03	514	MOV AL,BL		590	CHECK FOR HOT INTERRUPTS
E1DD AA	515	STOSB		591	-----
E1DE FECA	516	DEC DL		592	CLD
E1E0 75F6	517	JNC C22		593	MOV CX,8
E1E2 C03E	518	JNZ C23		594	MOV DI,OFFSET INT_PTR
E1E4 0E	519	PUSH CS		595	D3:
E1E5 17	520	POP SS		596	MOV AX,OFFSET D11
E1E6 FA	521	CLI		597	STOSB
E1E7 BC18E0	522	MOV SP,OFFSET C2		598	MOV AX,CODE
E1EA E202FE	523	JMP STGTEST		599	MOV AX,CODE
E1ED 7403	524	JE C25		600	STOSB
E1EF E900FE	525	JMP E901		601	ADD BX,4
	526			602	LOOP D3
	527	SETUP STACK SEG AND SP		603	INTERUPTS ARE MASKED OFF. CHECK THAT NO INTERRUPTS OCCUR.
	528			604	-----
	529			605	XOR AH,AH
E1FE	530	MOV AX,STACK		606	STI
E1FF B03000	531	MOV SS,AX		607	SUB CX,CX
E1FF 8000	532	MOV SP,OFFSET TOS		608	DA:
E1FF BC0001	533	MOV SP,OFFSET TOS		609	LOOP DS
	534	SETUP THE INT1 INTERRUPT VECTOR POINTER		610	DS:
	535			611	OR AH,AH
	536				

LOC OBJ	LINE	SOURCE
E270 7408	612	JZ 07
E270 7401	613	MOV DX,101H
E280 6A003	614	CALL ERR_BEEP
E283 FA	615	CLI
E294 F4	616	HLT
	617	-----
	618	TEST 7
	619	LODS DESCRIPTION
	620	VERIFY THAT THE SYSTEM TIMER (0) DOESN'T COUNT TOO FAST NOW TOO
	621	SLIM.
	622	-----
	623	OT:
E285	624	MOV AX,0
E285 B400	625	XOR CH,CH
E287 32E0	626	MOV AX,0
E288 B0FE	627	MOV AX,0
E288 E21	628	MOV AX,0
E288 B010	629	MOV AX,0
E288 E43	630	MOV AX,0
E291 B116	631	MOV AX,0
E293 8AC1	632	MOV AX,0
E295 E440	633	MOV AX,0
E297 FAC6FF	634	MOV AX,0
E29A 7554	635	MOV AX,0
E29C E2F9	636	MOV AX,0
E29E E2D0	637	MOV AX,0
E2A0 B112	638	MOV AX,0
E2A2 B0FF	639	MOV AX,0
E2A4 E440	640	MOV AX,0
E2A6 B400	641	MOV AX,0
E2A8 B0FE	642	MOV AX,0
E2AA E21	643	MOV AX,0
E2AC FAC6FF	644	MOV AX,0
E2AF 75CC	645	MOV AX,0
E2B1 E2F9	646	MOV AX,0
E2B3 E2A40	647	MOV AX,0
	648	-----
	649	TEMPORARY INTERRUPT SERVICE ROUTINE
	650	-----
	651	PROC NEAR
E2B6	652	MOV AX,1
E2B6 B401	653	PUSH AX
E2B8 50	654	MOV AX,0
E2B8 B0FF	655	MOV AX,0
E2B8 E21	656	MOV AX,0
E2B8 B020	657	MOV AX,0
E2B8 E440	658	MOV AX,0
E2C1 50	659	POP AX
E2C2 CF	660	IRET
	661	-----
E2C3	662	INT_INT PROC NEAR
E2C3 50	663	PUSH AX
E2C4 E440	664	IN AL,PORT_C
E2C4 A840	665	TEST AL,40H
E2C4 740A	666	JZ D12
E2C4 B19E2	667	MOV SI,OFFSET D1
E2C4 B9E000	668	MOV CX,D1L
E2C4 E20A	669	JMP SHORT D13
E2C4 E20A	670	D12:
E2C4 A840	671	TEST AL,40H
E2C4 7410	672	JZ D14
E2C4 BE27E2	673	MOV SI,OFFSET D2
E2C4 B9E000	674	MOV CX,D1L
E2C4	675	D13:
E2C4 B00000	676	MOV AX,0
E2C4 C010	677	INT 10H
E2C4 E2E603	678	CALL P_MSG
E2E4 FA	679	CLI
E2E5 F4	680	HLT
E2E6	681	D14:
E2E6 58	682	POP AX
E2E7 CF	683	IRET
	684	INT_INT ENDP

LOC OBJ	LINE	SOURCE
	685	-----
	686	INITIAL RELIABILITY TEST -- PHASE 3
	687	ASSUME CS:CODE,DS:DATA
	688	-----
E2E8 20323031	689	EI 00 '301'
0004	690	EI 00 4-EI
	691	-----
	692	ESTABLISH BIOS SUBROUTINE CALL INTERRUPT VECTORS
	693	-----
	694	TS10:
E2EC FC	695	CLO
E2ED DF4000	696	MOV DI,OFFSET VIDEO_INT
E2F0 0E	697	PUSH CS
E2F1 IF	698	POP DS
E2F2 0E13FF	699	MOV SI,OFFSET VIDEO_INT
E2F5 B92000	700	MOV CX,20H
E2F6 F3	701	REP MOVSB
E2F9 A5	702	REP MOVSB
	703	-----
	704	SETUP TIMER 0 TO MODE 3
	705	-----
E2FA B0FF	706	MOV AL,0FFH
E2FB E621	707	OUT INTR0,AL
E2FC B036	708	MOV AL,36H
E2FD E6A3	709	OUT INTR0,AL
E2FE B000	710	MOV AL,0
E2FF E6A0	711	OUT INTR0,AL
E300 E6A0	712	OUT INTR0,AL
E306 E6A0	713	OUT INTR0,AL
	714	-----
	715	SETUP TIMER 0 TO BLINK LED IF MANUFACTURING TEST MODE
	716	-----
E30A B0A000	717	MOV DS,DATA
E30B A000	718	MOV AX,DATA
E30D E27B03	719	CALL BIOS_RESET
E310 B0FBA3	720	CALL BIOS_RESET
E313 7426	721	JZ E3
E315 B03C	722	MOV AL,3CH
E317 E661	723	OUT PORT_B,AL
E319 90	724	MOV AL,0
E31A 90	725	MOV AL,0
E31B E6A0	726	OUT PORT_A,AL
E31D 24FF	727	AND AL,0FFH
E31F 7516	728	JNZ E2
E321 FE061200	729	INC HFG_TST
E325 26C796200B26	730	MOV ES:INT_ADDR+0FFH,INT
E32C 26C796200B26	731	MOV ES:INT_ADDR+2,0
E330 B0FE	732	MOV AL,0FFH
E335 E621	733	OUT INTR0,AL
E337	734	-----
E337 B0CC	735	MOV AL,0CH
E339 E661	736	OUT PORT_B,AL
	737	-----
	738	TEST 05
	739	-----
	740	ROS CHECKSUM II
	741	-----
	742	A CHECKSUM IS DONE FOR THE 4 ROS MODULES CONTAINING BASIC CODE
	743	-----
E339	743	E3:
E339 B204	744	MOV DL,4
E33D B0B000	745	MOV BX,0000H
E340 E60FE	746	CALL ROS_CHECKSUM
E343 7507	747	JNE E5
E345 FECA	748	DEC DL
E347 75F7	749	JNZ E4
E349 E00790	750	JMP E6
E34C	751	E5:
E34C B0A0101	752	MOV DX,101H
E34F E0B02	753	CALL ERR_BEEP
	754	-----

LOC OBJ	LINE	SOURCE	LOC OBJ	LINE	SOURCE
E352	755	TEST_08	E300	824	TEST_10 CRT INTERFACE LINES TEST
E353 E440	756	INITIALIZE AND START CRT CONTROLLER (69451)	E301 50	825	DESCRIPTION
E354 E400	757	TEST VIDEO READ/WRITE STORAGE.	E302 80FC30	826	SENSE ON/OFF TRANSITION OF THE VIDEO ENABLE AND HORIZONTAL
E355 A31000	758	RESET THE VIDEO ENABLE SIGNAL.	E303 AH,30H	827	STMC LINES.
E356 7409	759	SELECT ALPHANUMERIC MODE, 40 = 25, B & W.	E304 DX,030AH	828	POP AX
E357 FE00	760	READ/WRITE DATA PATT: 1105 TO STG. CHECK STG ADDRESSABILITY.	E305 JE E11	829	PUSH AX
E358 7503	761	TEST VIDEO TESTS FOR BURN-IN	E306 DX,030AH	830	POP AX
E359 E9800	762	TEST VIDEO.	E307 AH,B	831	SAVE IT
E360	763	TEST VIDEO.	E308 MOV AX	832	10/M CARD ATTACHED?
E361 A450	764	TEST VIDEO.	E309 CHP AH,30H	833	SETUP ADDR OF BN STATUS PORT
E362 80FC30	765	TEST VIDEO.	E310 DX,030AH	834	TEST - GO TEST LINES
E363 7409	766	TEST VIDEO.	E311 MOV DX,030AH	835	COLOR CARD IS ATTACHED
E364	767	TEST VIDEO.	E312 MOV AX	836	LINE TEST
E365 A450	768	TEST VIDEO.	E313 MOV AX,B	837	OF LOOP_CNT
E366 80FC30	769	TEST VIDEO.	E314 SUB CX,CX	838	READ CRT STATUS PORT
E367 7409	770	TEST VIDEO.	E315 IN AL,CX	839	CHECK VIDEO/HORZ LINE
E368 FE00	771	TEST VIDEO.	E316 AND AL,AH	840	IT'S ON - CHECK IF IT GOES OFF
E369 80FC20	772	TEST VIDEO.	E317 JNZ E14	841	DISPLAY TILL ON OR TIMEOUT
E370 7502	773	TEST VIDEO.	E318 LOOP E13	842	GO PRINT ERROR MSG
E371 8003	774	TEST VIDEO.	E319 JMP SHORT E17	843	READ CRT STATUS PORT
E372	775	TEST VIDEO.	E320 MOV CX,CX	844	CHECK VIDEO/HORZ LINE
E373 2AC4	776	TEST VIDEO.	E321 IN AL,DX	845	IT'S ON - CHECK NEXT LINE
E374 2AC4	777	TEST VIDEO.	E322 AND AL,AH	846	LOOP IF OFF TILL IT GOES ON
E375 50	778	TEST VIDEO.	E323 JNC E14	847	NOT LINE
E376 50	779	TEST VIDEO.	E324 JMP SHORT E17	848	GET NEXT BIT TO CHECK
E377 8000B0	780	TEST VIDEO.	E325 MOV CL,3	849	GO CHECK HORIZONTAL LINE
E378 8000B0	781	TEST VIDEO.	E326 SHR AH,CL	850	DISPLAY CURSOR ON SCREEN
E379 800010	782	TEST VIDEO.	E327 JNZ E12	851	CRT_ERR
E380 8001	783	TEST VIDEO.	E328 JMP SHORT E1B	852	GO BEEP SPEAKER
E381 80FC30	784	TEST VIDEO.	E329 MOV DX,102H	853	DISPLAY SENSE SHS (AH)
E382 740B	785	TEST VIDEO.	E330 CALL EPR_BEEP	854	SET MODE AND DISPLAY CURSOR
E383 8000B0	786	TEST VIDEO.	E331 POP AX	855	CALL VIDEO I/O PROCEDURE
E384 8000B0	787	TEST VIDEO.	E332 MOV AX,0	856	TEST_11
E385 800040	788	TEST VIDEO.	E333 MOV DX,AX	857	ADDITIONAL READ/WRITE STORAGE TEST
E386 FE00	789	TEST VIDEO.	E334 DEC AL	858	DESCRIPTION
E387	790	TEST VIDEO.	E335 OUT DX,AL	859	WRITE/READ DATA PATTERNS TO ANY READ/WRITE STORAGE AFTER THE BASIC
E388 EC	791	TEST VIDEO.	E336 MOV ES,BX	860	10K STORAGE ADDRESSABILITY IS CHECKED.
E389 EC3	792	TEST VIDEO.	E337 MOV AX,DATA	861	ASSUME DS:DATA
E390 8000	793	TEST VIDEO.	E338 MOV DS,AX	862	MOV AX,DATA
E391	794	TEST VIDEO.	E339 MOV DS,AX	863	DETERMINE RAM SIZE ON PLUJAR BOARD
E392	795	TEST VIDEO.	E340 MOV DS,AX	864	MOV AX,BYTE PTR EQUIP_FLAG
E393 EC3	796	TEST VIDEO.	E341 MOV DS,AX	865	ISOLATE RAM SIZE SHS
E394 8000	797	TEST VIDEO.	E342 MOV DS,AX	866	MOV DS,AX
E395 813E72003412	798	TEST VIDEO.	E343 MOV DS,AX	867	MOV DS,AX
E396 8000	799	TEST VIDEO.	E344 MOV DS,AX	868	MOV DS,AX
E397 8000	800	TEST VIDEO.	E345 MOV DS,AX	869	MOV DS,AX
E398 8000	801	TEST VIDEO.	E346 MOV DS,AX	870	MOV DS,AX
E399 8000	802	TEST VIDEO.	E347 MOV DS,AX	871	MOV DS,AX
E400 8000	803	TEST VIDEO.	E348 MOV DS,AX	872	MOV DS,AX
E401 8000	804	TEST VIDEO.	E349 MOV DS,AX	873	MOV DS,AX
E402 8000	805	TEST VIDEO.	E350 MOV DS,AX	874	MOV DS,AX
E403 8000	806	TEST VIDEO.	E351 MOV DS,AX	875	MOV DS,AX
E404 8000	807	TEST VIDEO.	E352 MOV DS,AX	876	MOV DS,AX
E405 8000	808	TEST VIDEO.	E353 MOV DS,AX	877	MOV DS,AX
E406 8000	809	TEST VIDEO.	E354 MOV DS,AX	878	MOV DS,AX
E407 8000	810	TEST VIDEO.	E355 MOV DS,AX	879	MOV DS,AX
E408 8000	811	TEST VIDEO.	E356 MOV DS,AX	880	MOV DS,AX
E409 8000	812	TEST VIDEO.	E357 MOV DS,AX	881	MOV DS,AX
E410 8000	813	TEST VIDEO.	E358 MOV DS,AX	882	MOV DS,AX
E411 8000	814	TEST VIDEO.	E359 MOV DS,AX	883	MOV DS,AX
E412 8000	815	TEST VIDEO.	E360 MOV DS,AX	884	MOV DS,AX
E413 8000	816	TEST VIDEO.	E361 MOV DS,AX	885	MOV DS,AX
E414 8000	817	TEST VIDEO.	E362 MOV DS,AX	886	MOV DS,AX
E415 8000	818	TEST VIDEO.	E363 MOV DS,AX	887	MOV DS,AX
E416 8000	819	TEST VIDEO.	E364 MOV DS,AX	888	MOV DS,AX
E417 8000	820	TEST VIDEO.	E365 MOV DS,AX	889	MOV DS,AX
E418 8000	821	TEST VIDEO.	E366 MOV DS,AX	890	MOV DS,AX
E419 8000	822	TEST VIDEO.	E367 MOV DS,AX	891	MOV DS,AX
E420 8000	823	TEST VIDEO.	E368 MOV DS,AX	892	MOV DS,AX
E421 8000	824	TEST VIDEO.	E369 MOV DS,AX	893	MOV DS,AX
E422 8000	825	TEST VIDEO.	E370 MOV DS,AX	894	MOV DS,AX
E423 8000	826	TEST VIDEO.	E371 MOV DS,AX	895	MOV DS,AX
E424 8000	827	TEST VIDEO.	E372 MOV DS,AX	896	MOV DS,AX
E425 8000	828	TEST VIDEO.	E373 MOV DS,AX	897	MOV DS,AX
E426 8000	829	TEST VIDEO.	E374 MOV DS,AX	898	MOV DS,AX
E427 8000	830	TEST VIDEO.	E375 MOV DS,AX	899	MOV DS,AX
E428 8000	831	TEST VIDEO.	E376 MOV DS,AX	900	MOV DS,AX
E429 8000	832	TEST VIDEO.	E377 MOV DS,AX	901	MOV DS,AX
E430 8000	833	TEST VIDEO.	E378 MOV DS,AX	902	MOV DS,AX
E431 8000	834	TEST VIDEO.	E379 MOV DS,AX	903	MOV DS,AX
E432 8000	835	TEST VIDEO.	E380 MOV DS,AX	904	MOV DS,AX
E433 8000	836	TEST VIDEO.	E381 MOV DS,AX	905	MOV DS,AX
E434 8000	837	TEST VIDEO.	E382 MOV DS,AX	906	MOV DS,AX
E435 8000	838	TEST VIDEO.	E383 MOV DS,AX	907	MOV DS,AX
E436 8000	839	TEST VIDEO.	E384 MOV DS,AX	908	MOV DS,AX
E437 8000	840	TEST VIDEO.	E385 MOV DS,AX	909	MOV DS,AX
E438 8000	841	TEST VIDEO.	E386 MOV DS,AX	910	MOV DS,AX
E439 8000	842	TEST VIDEO.	E387 MOV DS,AX	911	MOV DS,AX
E440 8000	843	TEST VIDEO.	E388 MOV DS,AX	912	MOV DS,AX
E441 8000	844	TEST VIDEO.	E389 MOV DS,AX	913	MOV DS,AX
E442 8000	845	TEST VIDEO.	E390 MOV DS,AX	914	MOV DS,AX
E443 8000	846	TEST VIDEO.	E391 MOV DS,AX	915	MOV DS,AX
E444 8000	847	TEST VIDEO.	E392 MOV DS,AX	916	MOV DS,AX
E445 8000	848	TEST VIDEO.	E393 MOV DS,AX	917	MOV DS,AX
E446 8000	849	TEST VIDEO.	E394 MOV DS,AX	918	MOV DS,AX
E447 8000	850	TEST VIDEO.	E395 MOV DS,AX	919	MOV DS,AX
E448 8000	851	TEST VIDEO.	E396 MOV DS,AX	920	MOV DS,AX
E449 8000	852	TEST VIDEO.	E397 MOV DS,AX	921	MOV DS,AX
E450 8000	853	TEST VIDEO.	E398 MOV DS,AX	922	MOV DS,AX
E451 8000	854	TEST VIDEO.	E399 MOV DS,AX	923	MOV DS,AX
E452 8000	855	TEST VIDEO.	E400 MOV DS,AX	924	MOV DS,AX
E453 8000	856	TEST VIDEO.	E401 MOV DS,AX	925	MOV DS,AX
E454 8000	857	TEST VIDEO.	E402 MOV DS,AX	926	MOV DS,AX
E455 8000	858	TEST VIDEO.	E403 MOV DS,AX	927	MOV DS,AX
E456 8000	859	TEST VIDEO.	E404 MOV DS,AX	928	MOV DS,AX
E457 8000	860	TEST VIDEO.	E405 MOV DS,AX	929	MOV DS,AX
E458 8000	861	TEST VIDEO.	E406 MOV DS,AX	930	MOV DS,AX
E459 8000	862	TEST VIDEO.	E407 MOV DS,AX	931	MOV DS,AX
E460 8000	863	TEST VIDEO.	E408 MOV DS,AX	932	MOV DS,AX
E461 8000	864	TEST VIDEO.	E409 MOV DS,AX	933	MOV DS,AX
E462 8000	865	TEST VIDEO.	E410 MOV DS,AX	934	MOV DS,AX
E463 8000	866	TEST VIDEO.	E411 MOV DS,AX	935	MOV DS,AX
E464 8000	867	TEST VIDEO.	E412 MOV DS,AX	936	MOV DS,AX
E465 8000	868	TEST VIDEO.	E413 MOV DS,AX	937	MOV DS,AX
E466 8000	869	TEST VIDEO.	E414 MOV DS,AX	938	MOV DS,AX
E467 8000	870	TEST VIDEO.	E415 MOV DS,AX	939	MOV DS,AX
E468 8000	871	TEST VIDEO.	E416 MOV DS,AX	940	MOV DS,AX
E469 8000	872	TEST VIDEO.	E417 MOV DS,AX	941	MOV DS,AX
E470 8000	873	TEST VIDEO.	E418 MOV DS,AX	942	MOV DS,AX
E471 8000	874	TEST VIDEO.	E419 MOV DS,AX	943	MOV DS,AX
E472 8000	875	TEST VIDEO.	E420 MOV DS,AX	944	MOV DS,AX
E473 8000	876	TEST VIDEO.	E421 MOV DS,AX	945	MOV DS,AX
E474 8000	877	TEST VIDEO.	E422 MOV DS,AX	946	MOV DS,AX
E475 8000	878	TEST VIDEO.	E423 MOV DS,AX	947	MOV DS,AX
E476 8000	879	TEST VIDEO.	E424 MOV DS,AX	948	MOV DS,AX
E477 8000	880	TEST VIDEO.	E425 MOV DS,AX	949	MOV DS,AX
E478 8000	881	TEST VIDEO.	E426 MOV DS,AX	950	MOV DS,AX
E479 8000	882	TEST VIDEO.	E427 MOV DS,AX	951	MOV DS,AX
E480 8000	883	TEST VIDEO.	E428 MOV DS,AX	952	MOV DS,AX
E481 8000	884	TEST VIDEO.	E429 MOV DS,AX	953	MOV DS,AX
E482 8000	885	TEST VIDEO.	E430 MOV DS,AX	954	MOV DS,AX
E483 8000	886	TEST VIDEO.	E431 MOV DS,AX	955	MOV DS,AX
E484 8000	887	TEST VIDEO.	E432 MOV DS,AX	956	MOV DS,AX
E485 8000	888	TEST VIDEO.	E433 MOV DS,AX	957	MOV DS,AX
E486 8000	889	TEST VIDEO.	E434 MOV DS,AX	958	MOV DS,AX
E487 8000	890	TEST VIDEO.	E435 MOV DS,AX	959	MOV DS,AX
E488 8000	891	TEST VIDEO.	E436 MOV DS,AX	960	MOV DS,AX
E489 8000	892	TEST VIDEO.	E437 MOV DS,AX	961	MOV DS,AX
E490 8000	893	TEST VIDEO.	E438 MOV DS,AX	962	MOV DS,AX
E491 8000	894	TEST VIDEO.	E439 MOV DS,AX	963	MOV DS,AX
E492 8000	895	TEST VIDEO.	E440 MOV DS,AX	964	MOV DS,AX
E493 8000	896	TEST VIDEO.	E441 MOV DS,AX	965	MOV DS,AX
E494 8000	897	TEST VIDEO.	E442 MOV DS,AX	966	MOV DS,AX
E495 8000	898	TEST VIDEO.	E443 MOV DS,AX	967	MOV DS,AX
E496 8000	899	TEST VIDEO.	E444 MOV DS,AX	968	MOV DS,AX
E497 8000	900	TEST VIDEO.	E445 MOV DS,AX	969	MOV DS,AX
E498 8000	901	TEST VIDEO.	E446 MOV DS,AX	970	MOV DS,AX
E499 8000	902	TEST VIDEO.	E447 MOV DS,AX	971	MOV DS,AX
E500 8000	903	TEST VIDEO.	E448 MOV DS,AX	972	MOV DS,AX
E501 8000	904	TEST VIDEO.	E449 MOV DS,AX	973	MOV DS,AX
E502 8000	905	TEST VIDEO.	E450 MOV DS,AX	974	MOV DS,AX
E503 8000	906	TEST VIDEO.	E451 MOV DS,AX	975	MOV DS,AX
E504 8000	907	TEST VIDEO.	E452 MOV DS,AX	976	MOV DS,AX
E505 8000	908	TEST VIDEO.	E453 MOV DS,AX	977	MOV DS,AX
E506 8000	909	TEST VIDEO.	E454 MOV DS,AX	978	MOV DS,AX
E507 8000	910	TEST VIDEO.	E455 MOV DS,AX	979	MOV DS,AX
E508 8000	911	TEST VIDEO.	E456 MOV DS,AX	980	MOV DS,AX
E509 8000	912	TEST VIDEO.	E457 MOV DS,AX	981	MOV DS,AX
E510 8000	913	TEST VIDEO.	E458 MOV DS,AX	982	MOV DS,AX
E511 8000	914	TEST VIDEO.	E459 MOV DS,AX	983	MOV DS,AX
E512 8000	915	TEST VIDEO.	E460 MOV DS,AX	984	MOV DS,AX
E513 8000	916	TEST VIDEO.	E461 MOV DS,AX	985	MOV DS,AX
E514 8000	917	TEST VIDEO.	E462 MOV DS,AX	986	MOV DS,AX
E515 8000	918	TEST VIDEO.	E463 MOV DS,AX	987	MOV DS,AX
E516 8000	919	TEST VIDEO.	E464 MOV DS,AX	988	MOV DS,AX
E517 8000	920	TEST VIDEO.	E465 MOV DS,AX	989	MOV DS,AX
E518 8000	921	TEST VIDEO.	E466 MOV DS,AX	990	MOV DS,AX
E519 8000	922	TEST VIDEO.	E467 MOV DS,AX	991	MOV DS,AX
E520 8000	923	TEST VIDEO.	E468 MOV DS,AX	992	MOV DS,AX
E521 8000	924	TEST VIDEO.	E469 MOV DS,AX	993	MOV DS,AX
E522 8000	925	TEST VIDEO.	E470 MOV DS,AX	994	MOV DS,AX
E523 8000	926	TEST VIDEO.	E471 MOV DS,AX	995	MOV DS,AX
E524 8000	927	TEST VIDEO.	E472 MOV DS,AX	996	MOV DS,AX
E525 8000	928	TEST VIDEO.	E473 MOV DS,AX	997	MOV DS,AX
E526 8000	929	TEST VIDEO.	E474 MOV DS,AX	998	MOV DS,AX
E527 8000	930	TEST VIDEO.	E475 MOV DS,AX	999	MOV DS,AX
E528 8000	931	TEST VIDEO.	E476 MOV DS,AX	1000	MOV DS,AX
E529 8000	932	TEST VIDEO.	E477 MOV DS,AX	1001	MOV DS,AX
E530 8000	933	TEST VIDEO.	E478 MOV DS,AX	1002	MOV DS,AX
E531 8000	934	TEST VIDEO.	E479 MOV DS,AX	1003	MOV DS,AX
E532 8000	935	TEST VIDEO.	E480 MOV DS,AX	1004	MOV DS,AX
E533 8000	936	TEST VIDEO.	E481 MOV DS,AX	1005	MOV DS,AX
E534 8000	937	TEST VIDEO.	E482 MOV DS,AX	1006	MOV DS,AX
E535 8000	938	TEST VIDEO.	E483 MOV DS,AX	1007	MOV DS,AX
E536 8000	939	TEST VIDEO.	E484 MOV DS,AX	1008	MOV DS,AX
E537 8000	940	TEST VIDEO.	E485 MOV DS,AX	1009	MOV DS,AX
E538 8000	941	TEST VIDEO.	E486 MOV DS,AX	1010	MOV DS,AX
E539 8000	942	TEST VIDEO.	E487 MOV DS,AX	1011	MOV DS,AX
E540 8000	943	TEST VIDEO.	E488 MOV DS,AX	1012	MOV DS,AX
E541 8000	944	TEST VIDEO.	E489 MOV DS,AX	1013	MOV DS,AX
E542 8000	945	TEST VIDEO.	E490 MOV DS,AX	1014	MOV DS,AX
E543 8000	946	TEST VIDEO.	E491 MOV DS,AX	1015	MOV DS,AX
E544 8000	947	TEST VIDEO.	E492 MOV DS,AX	1016	MOV DS,

LOC OBJ	LINE	SOURCE	LOC OBJ	LINE	SOURCE
E428 7440	900	JE E22		974	INITIAL RELIABILITY TEST -- PHASE 4
	901			975	ASSUME CS:CODE:DS:DATA
E429 840004	902	TEST ANY OTHER READ/WRITE STORAGE AVAILABLE		976	
E430 841000	903			977	
E431 841000	904	MOV BX,400H		978	F1 DB '301'
E432 841000	905	MOV CX,16		979	F1 EQU 9-F1
E433 841000	906			980	F2 DB '131'
E434 841000	907	MOV DX,CX		981	F2 EQU 9-F2
E435 7446	908	JBE E23		982	F3 DB '601'
E436 841000	909	MOV DS,BX		983	F3 EQU 9-F3
E437 841000	910	MOV ES,BX		984	F4 LABEL WORD
E438 841000	911	ADD CX,16		985	F4 LABEL WORD
E439 841000	912	ADD BX,400H		986	F4 LABEL WORD
E440 841000	913	PUSH CX		987	F4 LABEL WORD
E441 841000	914	PUSH BX		988	F4 LABEL WORD
E442 52	915	PUSH DX		989	F4 LABEL WORD
E443 841000	916	CALL STGTST		990	ASCII_TBL DB '0123456789ABCDEF'
E444 841000	917	POP DX		991	TEST:12
E445 841000	918	POP BX		992	KEYBOARD TEST
E446 841000	919	POP CX		993	DESCRIPTION
E447 841000	920	JE E21		994	RESET THE KEYBOARD AND CHECK THAT SCAN CODE 'A' IS RETURNED
	921	PRINT FAILING ADDRESS AND XOR'ED PATTERN IF DATA COMPARE ERROR		995	TO THE CPU. CHECK FOR STUCK KEYS.
E448 841000	922			996	
E449 841000	923	MOV DX,DS		997	TEST:12
E450 841000	924	MOV CH,AL		998	MOV AX,DATA
E451 841000	925	MOV AL,OH		999	MOV DS,AX
E452 841000	926	MOV CL,4		1000	MOV DS,AX
E453 841000	927	SHR AL,CL		1001	MOV DS,AX
E454 841000	928	CALL XLAT_PRINT_CODE		1002	JE F7
E455 841000	929	MOV AL,OH		1003	CALL XBD_RESET
E456 841000	930	MOV AL,OH		1004	CALL JCXZ F6
E457 841000	931	AND AL,0FH		1005	MOV AL,OH
E458 841000	932	CALL XLAT_PRINT_CODE		1006	OUT PORT_B,AL
E459 841000	933	MOV AL,CH		1007	CHP BL,0AH
E460 841000	934	SHR AL,CL		1008	JNE F6
E461 841000	935	CALL XLAT_PRINT_CODE		1009	MOV DS,AX
E462 841000	936	MOV AL,CH		1010	MOV DS,AX
E463 841000	937	MOV AL,OH		1011	MOV DS,AX
E464 841000	938	AND AL,0FH		1012	MOV DS,AX
E465 841000	939	CALL XLAT_PRINT_CODE		1013	MOV DS,AX
E466 841000	940	MOV SI,OFFSET E1		1014	MOV DS,AX
E467 841000	941	MOV CX,E1		1015	OUT PORT_B,AL
E468 841000	942	CALL P_MSG		1016	SUB CX,CX
E469 841000	943	JMP TEST12		1017	LOOP F5
E470 841000	944	JMP TEST12		1018	IN AL,KBD_IN
E471 841000	945	MOV DS,AX		1019	CHP AL,0
E472 841000	946	MOV DS,AX		1020	JE F7
E473 841000	947	MOV DS,AX		1021	MOV DS,AX
E474 841000	948	MOV DS,AX		1022	MOV DS,AX
E475 841000	949	MOV DS,AX		1023	MOV DS,AX
E476 841000	950	MOV DS,AX		1024	MOV DS,AX
E477 841000	951	MOV DS,AX		1025	MOV DS,AX
E478 841000	952	MOV DS,AX		1026	MOV DS,AX
E479 841000	953	MOV DS,AX		1027	MOV DS,AX
E480 841000	954	MOV DS,AX		1028	MOV DS,AX
E481 841000	955	MOV DS,AX		1029	MOV DS,AX
E482 841000	956	MOV DS,AX		1030	MOV DS,AX
E483 841000	957	MOV DS,AX		1031	MOV DS,AX
E484 841000	958	MOV DS,AX		1032	MOV DS,AX
E485 841000	959	MOV DS,AX		1033	MOV DS,AX
E486 841000	960	MOV DS,AX		1034	MOV DS,AX
E487 841000	961	MOV DS,AX		1035	MOV DS,AX
E488 841000	962	MOV DS,AX		1036	MOV DS,AX
E489 841000	963	MOV DS,AX		1037	MOV DS,AX
E490 841000	964	MOV DS,AX		1038	MOV DS,AX
E491 841000	965	MOV DS,AX		1039	MOV DS,AX
E492 841000	966	MOV DS,AX		1040	MOV DS,AX
E493 841000	967	MOV DS,AX		1041	MOV DS,AX
E494 841000	968	MOV DS,AX		1042	MOV DS,AX
E495 841000	969	MOV DS,AX		1043	MOV DS,AX
E496 841000	970	MOV DS,AX		1044	MOV DS,AX
E497 841000	971	MOV DS,AX		1045	MOV DS,AX
E498 841000	972	MOV DS,AX		1046	MOV DS,AX
E499 841000	973	MOV DS,AX		1047	MOV DS,AX

LOC OBJ	LINE	SOURCE	LOC OBJ	LINE	SOURCE
1045	1045	TEST 13	E595 E591	1122	MOV CH1
1046	1046	DISPOSITION	E597 M01A3E00	1123	R
1047	1047	CASSETTE DATA WRAP TEST	E598 E0F308	1124	CALL SEEK
1048	1048	TURN CASSETTE MOTOR OFF, WRITE A BIT OUT TO THE CASSETTE DATA BUS.	E599 7207	1125	JC F13
1049	1049	VERIFY THAT CASSETTE DATA READ IS WITHIN A VALID RANGE.	E59A B822	1126	MOV CH1
1050	1050	TURN THE CASSETTE MOTOR OFF	E59B E0E006	1127	CALL SEEK
1051	1051	WRITE A BIT	E59C 7309	1128	JNC F14
1052	1052	TURN THE CASSETTE MOTOR OFF	E597	1129	JMP
1053	1053	MOV AX,DATA	E597 BAE6E4	1130	MOV SI,OFFSET F3
1054	1054	MOV DS,AX	E59A 900300	1131	MOV CA,FIL
1055	1055	MOV AL,0-0H	E59B C8A01	1132	CALL P1MSG
1056	1056	OUT PORT_0,AL	E59C	1133	TURN DRIVE 0 MOTOR OFF
1057	1057	WRITE A BIT	E5A0	1134	F14:
1058	1058	MOV AL,OFFH	E5A0 B00C	1135	MOV AL,0-0H
1059	1059	MOV AL,0-0H	E5A2 BAF203	1136	MOV DX,03F2H
1060	1060	MOV AL,0-0H	E5A3 EE	1137	OUT DX,AL
1061	1061	MOV AL,0-0H	E5A4	1138	SETUP PRINTER AND RS232 BASE ADDRESSES IF DEVICE ATTACHED
1062	1062	MOV AL,0-0H	E5A6	1141	F15:
1063	1063	MOV AL,0-0H	E5A6 C7061A01E00	1143	MOV BUFFER,HEAD,OFFSET KB_BUFFER
1064	1064	MOV AL,0-0H	E5A8 C7061C001E00	1144	MOV BUFFER,TAIL,OFFSET KB_BUFFER
1065	1065	MOV AL,0-0H	E5A2 B0B1E4	1145	MOV BP,OFFSET F4
1066	1066	MOV AL,0-0H	E5A5 RE0000	1147	MOV SI,0
1067	1067	MOV AL,0-0H	E5A6 2E8B5A00	1148	MOV DX,CS:BP1
1068	1068	MOV AL,0-0H	E5B0 B0A4	1149	MOV AL,0-0H
1069	1069	MOV AL,0-0H	E5B0 EE	1150	MOV AL,0-0H
1070	1070	MOV AL,0-0H	E5B0 2A00	1151	OUT DX,AL
1071	1071	MOV AL,0-0H	E5B1 EC	1152	SUB AL,AL
1072	1072	MOV AL,0-0H	E5B2 3E4	1153	JM AL,DX
1073	1073	MOV AL,0-0H	E5B3 3E4	1154	MOV AL,0-0H
1074	1074	MOV AL,0-0H	E5B4 7506	1155	JMP F17
1075	1075	MOV AL,0-0H	E5B5 099A0000	1156	MOV PRINTER_BASE,111,0X
1076	1076	MOV AL,0-0H	E5C4 46	1157	JNC SI
1077	1077	MOV AL,0-0H	E5C4 46	1158	JNC SI
1078	1078	MOV AL,0-0H	E5C4 46	1159	JNC SI
1079	1079	MOV AL,0-0H	E5C4 46	1160	JNC SI
1080	1080	MOV AL,0-0H	E5C4 46	1161	JNC SI
1081	1081	MOV AL,0-0H	E5C4 46	1162	JNC SI
1082	1082	MOV AL,0-0H	E5C4 46	1163	JNC SI
1083	1083	MOV AL,0-0H	E5C4 46	1164	JNC SI
1084	1084	MOV AL,0-0H	E5C4 46	1165	JNC SI
1085	1085	MOV AL,0-0H	E5C4 46	1166	JNC SI
1086	1086	MOV AL,0-0H	E5C4 46	1167	JNC SI
1087	1087	MOV AL,0-0H	E5C4 46	1168	JNC SI
1088	1088	MOV AL,0-0H	E5C4 46	1169	JNC SI
1089	1089	MOV AL,0-0H	E5C4 46	1170	JNC SI
1090	1090	MOV AL,0-0H	E5C4 46	1171	JNC SI
1091	1091	MOV AL,0-0H	E5C4 46	1172	JNC SI
1092	1092	MOV AL,0-0H	E5C4 46	1173	JNC SI
1093	1093	MOV AL,0-0H	E5C4 46	1174	JNC SI
1094	1094	MOV AL,0-0H	E5C4 46	1175	JNC SI
1095	1095	MOV AL,0-0H	E5C4 46	1176	JNC SI
1096	1096	MOV AL,0-0H	E5C4 46	1177	JNC SI
1097	1097	MOV AL,0-0H	E5C4 46	1178	JNC SI
1098	1098	MOV AL,0-0H	E5C4 46	1179	JNC SI
1099	1099	MOV AL,0-0H	E5C4 46	1180	JNC SI
1100	1100	MOV AL,0-0H	E5C4 46	1181	JNC SI
1101	1101	MOV AL,0-0H	E5C4 46	1182	JNC SI
1102	1102	MOV AL,0-0H	E5C4 46	1183	JNC SI
1103	1103	MOV AL,0-0H	E5C4 46	1184	JNC SI
1104	1104	MOV AL,0-0H	E5C4 46	1185	JNC SI
1105	1105	MOV AL,0-0H	E5C4 46	1186	JNC SI
1106	1106	MOV AL,0-0H	E5C4 46	1187	J

LINE	SOURCE	LOC OBJ	LINE	SOURCE
1199	R	6603 003E120001	1275	OUT PORT_B,AL
1200		6608 7406	1276	RET
1201		661A 0A0100	1277	BEEP ENDP
1202		661D 601000	1279	THIS PROCEDURE WILL SEND A SOFTWARE RESET TO THE KEYBOARD.
1203		6620	1280	! SCAN CODE 'AA' SHOULD BE RETURNED TO THE CPU.
1204		6620 09CF00	1281	!-----
1205		6623	1282	KBD_RESET PROC NEAR
1206	R	6623 003E120001	1283	MOV AL,0CH
1207		662A 7503	1284	OUT PORT_B,AL
1208		662A 092EFA	1285	MOV CX,10582
1209		662D	1286	MOV GA
1210		662D 0976FF	1287	MOV AL,0CH
1211			1288	OUT PORT_B,AL
1212			1289	SP_TEST: ! ENTRY FOR MANUFACTURING TEST 2
1213			1290	MOV AL,4CH
1214			1291	OUT PORT_B,AL
1215			1292	MOV AL,0FH
1216			1293	OUT PORT_B,AL
1217			1294	MOV AL,0
1218			1295	MOV CX,CX
1219			1296	SUB AN,OFFH
1220			1297	JLZ G10
1221			1298	LOOP G9
1222			1299	G10: !M
1223			1300	MOV BL,AL
1224			1301	MOV AL,0CH
1225			1302	OUT PORT_B,AL
1226			1303	RET
1227			1304	KBD_RESET ENDP
1228			1305	! BLINK LED PROCEDURE FOR MFG BURN-IN AND RUN-IN TESTS
1229	R	6633 004000	1307	! (LED WILL BLINK APPROXIMATELY .25 SECOND)
1230		6636 0E08	1309	BLINK_INT PROC NEAR
1231		6638 0AF6	1310	BLINK_INT PROC NEAR
1232		663A 7410	1311	MOV CX
1233		663C	1312	PUSH AX
1234		663C 0306	1313	IN AL,PORT_B
1235		663E 0A5500	1314	AND AL,0FH
1236		6641 02FE	1315	OUT PORT_B,AL
1237		6643 FEEC	1316	SUB CX,CX
1238		6645 75F5	1317	LOOP G11
1239	R	6647 003E120001	1318	MOV AL,40H
1240		664C 7506	1319	OUT PORT_B,AL
1241		664E 0A00	1320	MOV AL,01
1242		6650 0661	1321	OUT PORT_B,AL
1243		6652 0E08	1322	MOV AX
1244		6654	1323	POP CX
1245		6654 0301	1324	RET
1246		6656 0E0000	1325	BLINK_INT ENDP
1247		6659 02FE	1326	! THIS SUBROUTINE WILL PRINT A MESSAGE ON THE DISPLAY
1248		665B 0E0A	1327	!-----
1249		665D 75F5	1328	! ENTRY REQUIREMENTS:
1250		665F 02FE	1329	! SI = OFFSET ADDRESS OF MESSAGE BUFFER
1251		6661 02FE	1330	! CX = MESSAGE BYTE COUNT
1252		6663 0E03	1331	! MAXIMUM MESSAGE LENGTH IS 3A CHARACTERS
1253		6664 00	1332	!-----
1254		6665 C3	1333	P_MSG PROC NEAR
1255			1334	MOV AX,DATA
1256			1335	MOV DS,AX
1257			1336	MOV CX,1
1258		6666 0006	1337	MOV AX,DATA
1259		6668 0006	1338	MOV AX,DATA
1260		666A 0006	1339	MOV AX,DATA
1261		666B 0006	1340	MOV AX,DATA
1262		666C 0006	1341	MOV AX,DATA
1263		666D 0006	1342	MOV AX,DATA
1264		666E 0006	1343	MOV AX,DATA
1265		666F 0006	1344	MOV AX,DATA
1266		6670 0006	1345	MOV AX,DATA
1267		6671 0006	1346	MOV AX,DATA
1268		6672 0006	1347	MOV AX,DATA
1269		6673 0006	1348	MOV AX,DATA
1270		6674 0006	1349	MOV AX,DATA
1271		6675 0006	1350	MOV AX,DATA
1272		6676 0006		
1273		6677 0006		
1274		6678 0006		

LOC OBJ	LINE	SOURCE	LOC OBJ	LINE	SOURCE
E6F0 B80A0E	1351	MOV AX,REGM		1428	J
E6F0 CD10	1352	TUT 10H		1429	ON RETURN, CONDITIONS SET AS IN CALL TO COMPO STATUS (AH=3)
E6F1 C3	1353	RET		1430	SEND THE CHARACTER IN (AL) OVER THE COMPO LINE
	1354	P_PUSH		1431	(AH)=1 REGISTER IS PRESERVED
	1355	INT 19		1432	ON EXIT, BIT 7 OF AH IS SET IF THE ROUTINE WAS UNABLE TO
	1356	BOOT STRAP LOADER		1433	TRANSMIT THE BYTE OF DATA OVER THE LINE. THE
	1357	IF A 5 1/4" DISKETTE DRIVE IS AVAILABLE		1434	REMAINDER OF AH IS SET AS IN A STATUS REQUEST.
	1358	ON THE SYSTEM, TRACK 0, SECTOR 1 IS READ INTO THE		1435	REFLECTING THE CURRENT STATUS OF THE LINE.
	1359	BOOT LOCATION (SECTOR 0, OFFSET 7C00)		1436	(AH)=2 RECEIVE A CHARACTER IN (AL) FROM COMPO LINE BEFORE
	1360	AID CONTROL IS TRANSFERRED THERE.		1437	RETURNING TO CALLER
	1361			1438	ON EXIT, AH HAS THE CURRENT LINE STATUS, AS SET BY THE
	1362	IF THERE IS NO DISKETTE DRIVE, OR IF THERE IS		1439	THE STATUS ROUTINE, EXCEPT THAT THE ONLY BITS
	1363	IS A HARDWARE ERROR CONTROL IS TRANSFERRED		1440	LEFT ON ARE THE ERROR BITS (7,4,3,2,1)
	1364	TO THE CASSETTE BASIC ENTRY POINT.		1441	IN THIS CASE, THE TIME OUT BIT INDICATES DATA SET
	1365	IPL ASSUMPTIONS		1442	READY WAS NOT RECEIVED.
	1366	8255 PORT 60H BIT 0		1443	THUS, AH IS NON ZERO ONLY WHEN AN ERROR OCCURRED.
	1367	= 1 IF IPL FROM DISKETTE		1444	(AH)=3 RETURN THE COMPO PORT STATUS IN (AX)
	1368	ASSUME CS:CODE,DS:DATA		1445	AH CONTAINS THE LINE CONTROL STATUS
	1369	BOOT STRAP PROC NEAR		1446	BIT 7 = TIME OUT
E6F2	1370			1447	BIT 6 = TRANS SHIFT REGISTER EMPTY
E6F2 FB	1371	STI		1448	BIT 4 = BREAK DETECT
E6F2 B40000	1372	MOV AX,DATA		1449	BIT 3 = PARITY ERROR
E6F6 B0E0A	1373	MOV DS,AX		1450	BIT 2 = PARITY ERROR
E6F6 411000	1374	MOV AX,GROUP_FLAG		1451	BIT 1 = OVERRUN ERROR
E6F6 4001	1375	TEST AL,1		1452	BIT 0 = DATA READY
E6F6 7423	1376	JZ H3		1453	AL CONTAINS THE MODERN STATUS
	1377			1454	BIT 7 = RECEIVED LINE SIGNAL DETECT
	1378			1455	BIT 6 = RING INDICATOR
	1379			1456	BIT 5 = DATA SET READY
	1380			1457	BIT 4 = CLEAR TO SEND
E6F7 B00A00	1381			1458	BIT 3 = DELTA RECEIVE LINE SIGNAL DETECT
E702	1382	MOV CX,4		1459	BIT 2 = TRAILING EDGE RING DETECTOR
E702 51	1383	PUSH CX		1460	BIT 1 = DELTA DATA SET READY
E702 B4000	1384	MOV AH,0		1461	BIT 0 = DELTA CLEAR TO SEND
E702 CD13	1385	INT 13H		1462	(DX) = PARAMETER INDICATING WHICH RS232 CARD (0-1 ALLOWED)
E707 7214	1386	JC H2		1463	DATA AREA RS232_BASE CONTAINS THE BASE ADDRESS OF THE 8250 ON THE CARD
E707 8402	1387	MOV AH,2		1464	LOCATION 400H CONTAINS UP TO 4 RS232 ADDRESSES POSSIBLE
E708 B00000	1388	MOV BX,0		1465	OUTPUT
E708 86C3	1389	MOV ES,BX		1466	AX MODIFIED ACCORDING TO PARMS OF CALL
E710 88007C	1390	MOV BX,OFFSET BOOT_LOCH		1467	ALL OTHERS UNCHANGED
E710 B40000	1391	MOV DX,0		1468	ASSUME CS:CODE,DS:DATA
E716 B90100	1392	MOV CX,1		1469	AI LABEL WORD
E719 B001	1393	MOV AL,1		1470	DM 1067 ; 110 BAUD ; TABLE OF INIT VALUE
E719 C013	1394	INT 13H		1471	DM 768 ; 120
E71D 59	1395	POP CX		1472	DM 384 ; 300
E71E 7304	1396	JNC H4		1473	DM 192 ; 600
E720 E2E0	1397	LOOP H1		1474	DM 96 ; 1200
	1398			1475	DM 48 ; 2400
	1399			1476	DM 24 ; 4800
	1400			1477	DM 12 ; 9600
E722	1401			1478	
E722 CD1B	1402	INT 18H		1479	
	1403			1480	
	1404			1481	
	1405			1482	
E724	1406			1483	
E724 E4007C0000	1407	JMP BOOT_LOCH		1484	
	1408			1485	
	1409	BOOT_STRAP ENDP		1486	
	1410	RS232_IO		1487	
	1411			1488	
	1412			1489	
	1413			1490	
	1414			1491	
	1415			1492	
	1416			1493	
	1417			1494	
	1418			1495	
	1419			1496	
	1420			1497	
	1421			1498	
	1422			1499	
	1423			1500	
	1424			1501	
	1425			1502	
	1426			1503	
	1427			1504	

LOC OBJ	LINE	SOURCE	LOC OBJ	LINE	SOURCE
E75F	1505	A2: DEC A4	E7D1 EC	1502	IN AL-DX
E75F FECC	1506	JNZ A5	E7D2 A820	1503	TEST AL-20H
E761 7503	1507	JMP A10	E7D4 7500	1504	JNZ A11
E763 E9B00	1508		E7D6 7500	1505	LOOP A10
E764	1509	A3: POP CX	E7D8 83	1506	POP AX
E764 59	1510	POP DI	E7D9 80CC00	1507	DR AH-80H
E767 5F	1511	POP SI	E7DC E880	1508	JMP A3
E768 5E	1512	POP DX	E7DE	1509	A11: SUB DX-5
E769 5A	1513	POP DS	E7E0 03E005	1510	POP CX
E76A 1F	1514	IN	E7E1 59	1511	POP AX
E76B CF	1515	IN	E7E2 84C1	1512	POP AL-CL
	1516		E7E4 FE	1513	OUT DX-AL
	1517	----- INITIALIZE THE COMMUNICATIONS PORT	E7E5 E7E7FF	1514	JMP A3
	1518			1515	----- RECEIVE CHARACTER FROM COMPO LINE
E76C	1519	A4: MOV AH,AL	E7E6	1516	A12: AND BIOS_BREAK,37FH
E76C 84E0	1520	ADD DX-3	E7E6 80E671007F	1517	R
E76E 83C203	1521	MOV AL-80H	E7E8 53C204	1518	MOV DX-4
E771 B0B0	1522	OUT DX-AL	E7E9 B001	1519	MOV AL-1
E773 EE	1523		E7F2 EE	1520	OUT DX-AL
	1524	----- DETERMINE BAUD RATE DIVISOR	E7F3 53C202	1521	ADD DX-2
	1525		E7F5 28C9	1522	SUB CX-CX
E77A B0D4	1526	ROL DL-1	E7F6	1523	A13: MOV AL-DX
E77A D0C2	1527	ROL DL-1	E7F8 EC	1524	TEST AL-20H
E77B D0C2	1528	ROL DL-1	E7F9 A820	1525	TEST AL-20H
E77C D0C2	1529	ROL DL-1	E7FB 7507	1526	JNZ A15
E77E 81E2E000	1530	AND DX-8EH	E7FD E2F9	1527	LOOP A13
E782 B7267	1531	MOV DI-OFFSET A1	E7FF	1528	A14: MOV AH-80H
E785 03FA	1532	ADD DI-DX	E7FF 8400	1529	MOV AX-80H
E787 06940000	1533	MOV DX-PS232_BASE+1	E801 E427FF	1530	JMP A3
E788 42	1534	INC DX	E804 4A	1531	DEC DX
E78C 2E84A501	1535	MOV AL-CX:1011+1	E805 EC	1532	A15: MOV AL-DX
E790 EE	1536	OUT DX-AL	E806 4001	1533	TEST AL-1
E791 4A	1537	DEC DX	E808 7509	1534	JNZ A17
E792 2E8405	1538	MOV AL-CX:1011	E80A F686710800	1535	R
E795 EE	1539	OUT DX-AL	E80F 7474	1536	MOV AL-1
E796 84C4	1540	ADD DX-3	E811 E8BC	1537	JMP A14
E799 84C4	1541	MOV AL-AH	E813 841E	1538	MOV AL-00111100
E79B 241F	1542	AND AL-D1FH	E815 84C0	1539	MOV AH-AL
E79D EE	1543	AND AL-D1FH	E817 804D0000	1540	MOV DX-PS232_BASE+1
E79E 83E02	1544	SUB DX-2	E818 EC	1541	IN AL-DX
E7A1 B0B0	1545	MOV AL-0	E81C E477FF	1542	JMP A3
E7A3 EE	1546	OUT DX-AL		1543	----- COMPO PORT STATUS ROUTINE
E7A6 E878	1547	JMP SHORT A16		1544	A16: MOV DX-PS232_BASE+1
	1548			1545	ADD DX-5
	1549			1546	IN AL-DX
	1550			1547	MOV AH-AL
E7A6	1551	A5: PUSH AX		1548	INC DX
E7A6 59	1552	ADD DX-4		1549	IN AL-DX
E7A7 83C204	1553	POP AL-3		1550	TEST BIOS_BREAK,80H
E7A8 B003	1554	OUT DX-AL		1551	JZ A16
E7AC EE	1555	XOR CX-CX		1552	JMP A14
E7AD 33C9	1556	ADD DX-2		1553	A17: AND AL-00111100
E7AF 83C202	1557	MOV AL-DX		1554	MOV AH-AL
E7B2 EC	1558	TEST AL-20H		1555	MOV DX-PS232_BASE+1
E7B3 A820	1559	JNZ A7		1556	IN AL-DX
E7B5 7500	1560	LOOP A6		1557	MOV AH-AL
E7B7 E2F9	1561	POP AX		1558	INC DX
E7B9 50	1562	OR AH-80		1559	IN AL-DX
E7BA 0CC50	1563	JMP A3		1560	JMP A3
E7BB E8A7	1564	SUB CX-CX		1561	ENDP
E7BF	1565			1562	----- INT 16
E7C1 2B09	1566	MOV AL-DX		1563	----- THESE ROUTINES PROVIDE KEYBOARD SUPPORT
E7C1 EC	1567	TEST AL-10H		1564	1: KEYBOARD I/O
E7C2 A810	1568	JNZ A9		1565	1: INPUT
E7C4 7500	1569	LOOP A8		1566	1: READ THE NEXT ASCII CHARACTER STRUCK FROM THE KEYBOARD
E7C6 E2F9	1570	POP AX		1567	1: RETURN THE RESULT IN (AL), SCAN CODE IN (AH)
E7C8 50	1571	OR AH-80H		1568	1: SET THE X FLAG TO INDICATE IF AN ASCII CHARACTER IS AVAILABLE
E7C9 0CC50	1572	JMP A3		1569	1: TO BE READ.
E7CB E808	1573	SUB CX-CX		1570	1: (ZF)=1 -- NO CODE AVAILABLE
E7CD	1574			1571	1: (ZF)=0 -- CODE IS AVAILABLE
E7CE	1575			1572	1: IF ZF = 0, THE NEXT CHARACTER IN THE BUFFER TO BE READ IS
E7CF	1576			1573	1: IN AH, AND THE ENTRY REMAINS IN THE BUFFER
E7D0	1577			1574	1: RETURN THE CURRENT SHIFT STATUS IN AL REGISTER
E7D1	1578			1575	1: THE BIT SETTINGS FOR THIS CODE ARE INDICATED IN THE
E7D2	1579			1576	1: THE EQUATES FOR MB_FLAG
E7D3	1580			1577	1: OUTPUT
E7D4	1581			1578	1: AS NOTED ABOVE, ONLY AX AND FLAGS CHANGED
E7D5				1579	1: ALL REGISTERS RETAINED
E7D6				1580	1:-----
E7D7				1581	1:-----

LOC OBJ	LINE	SOURCE	LOC OBJ	LINE	SOURCE
E80E	1659	ASSUME CS:CODE DS:DATA	E80E	1736	DB CAPS_SHIFT,AM,SHIFT,SCROLL_SHIFT,ALT_SHIFT,CTL_SHIFT
E80F	1660	KEYBOARD_IO PROC FAR	E80F	1737	DB LEFT_SHIFT,RIGHT_SHIFT
E810	1661	INTERRUPTS BACK ON	E810	1738	DB
E811	1662	SAVE CURRENT DS	E811	1739	DB
E812	1663	SAVE BX TEMPORARILY	E812	1740	DB
E813	1664	MOV BX,DATA	E813	1741	DB
E814	1665	MOV DS,BX	E814	1742	DB
E815	1666	DR AM,AM	E815	1743	DB
E816	1667	JZ K1	E816	1744	DB
E817	1668	DEC AM	E817	1745	DB
E818	1669	JZ K2	E818	1746	DB
E819	1670	DEC AM	E819	1747	DB
E81A	1671	JZ K3	E81A	1748	DB
E81B	1672	POP BX	E81B	1749	DB
E81C	1673	POP DS	E81C	1750	DB
E81D	1674	IRET	E81D	1751	DB
E81E	1675	IRET	E81E	1752	DB
E81F	1676	IRET	E81F	1753	DB
E820	1677	IRET	E820	1754	DB
E821	1678	IRET	E821	1755	DB
E822	1679	IRET	E822	1756	DB
E823	1680	IRET	E823	1757	DB
E824	1681	IRET	E824	1758	DB
E825	1682	IRET	E825	1759	DB
E826	1683	IRET	E826	1760	DB
E827	1684	IRET	E827	1761	DB
E828	1685	IRET	E828	1762	DB
E829	1686	IRET	E829	1763	DB
E82A	1687	IRET	E82A	1764	DB
E82B	1688	IRET	E82B	1765	DB
E82C	1689	IRET	E82C	1766	DB
E82D	1690	IRET	E82D	1767	DB
E82E	1691	IRET	E82E	1768	DB
E82F	1692	IRET	E82F	1769	DB
E830	1693	IRET	E830	1770	DB
E831	1694	IRET	E831	1771	DB
E832	1695	IRET	E832	1772	DB
E833	1696	IRET	E833	1773	DB
E834	1697	IRET	E834	1774	DB
E835	1698	IRET	E835	1775	DB
E836	1699	IRET	E836	1776	DB
E837	1700	IRET	E837	1777	DB
E838	1701	IRET	E838	1778	DB
E839	1702	IRET	E839	1779	DB
E83A	1703	IRET	E83A	1780	DB
E83B	1704	IRET	E83B	1781	DB
E83C	1705	IRET	E83C	1782	DB
E83D	1706	IRET	E83D	1783	DB
E83E	1707	IRET	E83E	1784	DB
E83F	1708	IRET	E83F	1785	DB
E840	1709	IRET	E840	1786	DB
E841	1710	IRET	E841	1787	DB
E842	1711	IRET	E842	1788	DB
E843	1712	IRET	E843	1789	DB
E844	1713	IRET	E844	1790	DB
E845	1714	IRET	E845	1791	DB
E846	1715	IRET	E846	1792	DB
E847	1716	IRET	E847	1793	DB
E848	1717	IRET	E848	1794	DB
E849	1718	IRET	E849	1795	DB
E84A	1719	IRET	E84A	1796	DB
E84B	1720	IRET	E84B	1797	DB
E84C	1721	IRET	E84C	1798	DB
E84D	1722	IRET	E84D	1799	DB
E84E	1723	IRET	E84E	1800	DB
E84F	1724	IRET	E84F	1801	DB
E850	1725	IRET	E850	1802	DB
E851	1726	IRET	E851	1803	DB
E852	1727	IRET	E852	1804	DB
E853	1728	IRET	E853	1805	DB
E854	1729	IRET	E854	1806	DB
E855	1730	IRET	E855	1807	DB
E856	1731	IRET	E856	1808	DB
E857	1732	IRET	E857	1809	DB
E858	1733	IRET	E858	1810	DB
E859	1734	IRET	E859	1811	DB
E85A	1735	IRET	E85A	1812	DB
E85B	1736	IRET	E85B	1813	DB
E85C	1737	IRET	E85C	1814	DB
E85D	1738	IRET	E85D	1815	DB
E85E	1739	IRET	E85E	1816	DB
E85F	1740	IRET	E85F	1817	DB
E860	1741	IRET	E860	1818	DB
E861	1742	IRET	E861	1819	DB
E862	1743	IRET	E862	1820	DB
E863	1744	IRET	E863	1821	DB
E864	1745	IRET	E864	1822	DB
E865	1746	IRET	E865	1823	DB
E866	1747	IRET	E866	1824	DB
E867	1748	IRET	E867	1825	DB
E868	1749	IRET	E868	1826	DB
E869	1750	IRET	E869	1827	DB
E86A	1751	IRET	E86A	1828	DB
E86B	1752	IRET	E86B	1829	DB
E86C	1753	IRET	E86C	1830	DB
E86D	1754	IRET	E86D	1831	DB
E86E	1755	IRET	E86E	1832	DB
E86F	1756	IRET	E86F	1833	DB
E870	1757	IRET	E870	1834	DB
E871	1758	IRET	E871	1835	DB
E872	1759	IRET	E872	1836	DB
E873	1760	IRET	E873	1837	DB
E874	1761	IRET	E874	1838	DB
E875	1762	IRET	E875	1839	DB
E876	1763	IRET	E876	1840	DB
E877	1764	IRET	E877	1841	DB
E878	1765	IRET	E878	1842	DB
E879	1766	IRET	E879	1843	DB
E87A	1767	IRET	E87A	1844	DB
E87B	1768	IRET	E87B	1845	DB
E87C	1769	IRET	E87C	1846	DB
E87D	1770	IRET	E87D	1847	DB
E87E	1771	IRET	E87E	1848	DB
E87F	1772	IRET	E87F	1849	DB
E880	1773	IRET	E880	1850	DB
E881	1774	IRET	E881	1851	DB
E882	1775	IRET	E882	1852	DB
E883	1776	IRET	E883	1853	DB
E884	1777	IRET	E884	1854	DB
E885	1778	IRET	E885	1855	DB
E886	1779	IRET	E886	1856	DB
E887	1780	IRET	E887	1857	DB
E888	1781	IRET	E888	1858	DB
E889	1782	IRET	E889	1859	DB
E88A	1783	IRET	E88A	1860	DB
E88B	1784	IRET	E88B	1861	DB
E88C	1785	IRET	E88C	1862	DB
E88D	1786	IRET	E88D	1863	DB
E88E	1787	IRET	E88E	1864	DB
E88F	1788	IRET	E88F	1865	DB
E890	1789	IRET	E890	1866	DB
E891	1790	IRET	E891	1867	DB
E892	1791	IRET	E892	1868	DB
E893	1792	IRET	E893	1869	DB
E894	1793	IRET	E894	1870	DB
E895	1794	IRET	E895	1871	DB
E896	1795	IRET	E896	1872	DB
E897	1796	IRET	E897	1873	DB
E898	1797	IRET	E898	1874	DB
E899	1798	IRET	E899	1875	DB
E89A	1799	IRET	E89A	1876	DB
E89B	1800	IRET	E89B	1877	DB
E89C	1801	IRET	E89C	1878	DB
E89D	1802	IRET	E89D	1879	DB
E89E	1803	IRET	E89E	1880	DB
E89F	1804	IRET	E89F	1881	DB
E8A0	1805	IRET	E8A0	1882	DB
E8A1	1806	IRET	E8A1	1883	DB
E8A2	1807	IRET	E8A2	1884	DB
E8A3	1808	IRET	E8A3	1885	DB
E8A4	1809	IRET	E8A4	1886	DB
E8A5	1810	IRET	E8A5	1887	DB
E8A6	1811	IRET	E8A6	1888	DB
E8A7	1812	IRET	E8A7	1889	DB
E8A8	1813	IRET	E8A8	1890	DB
E8A9	1814	IRET	E8A9	1891	DB
E8AA	1815	IRET	E8AA	1892	DB
E8AB	1816	IRET	E8AB	1893	DB
E8AC	1817	IRET	E8AC	1894	DB
E8AD	1818	IRET	E8AD	1895	DB
E8AE	1819	IRET	E8AE	1896	DB
E8AF	1820	IRET	E8AF	1897	DB
E8B0	1821	IRET	E8B0	1898	DB
E8B1	1822	IRET	E8B1	1899	DB
E8B2	1823	IRET	E8B2	1900	DB
E8B3	1824	IRET	E8B3	1901	DB
E8B4	1825	IRET	E8B4	1902	DB
E8B5	1826	IRET	E8B5	1903	DB
E8B6	1827	IRET	E8B6	1904	DB
E8B7	1828	IRET	E8B7	1905	DB
E8B8	1829	IRET	E8B8	1906	DB
E8B9	1830	IRET	E8B9	1907	DB
E8BA	1831	IRET	E8BA	1908	DB
E8BB	1832	IRET	E8BB	1909	DB
E8BC	1833	IRET	E8BC	1910	DB
E8BD	1834	IRET	E8BD	1911	DB
E8BE	1835	IRET	E8BE	1912	DB
E8BF	1836	IRET	E8BF	1913	DB
E8C0	1837	IRET	E8C0	1914	DB
E8C1	1838	IRET	E8C1	1915	DB
E8C2	1839	IRET	E8C2	1916	DB
E8C3	1840	IRET	E8C3	1917	DB
E8C4	1841	IRET	E8C4	1918	DB
E8C5	1842	IRET	E8C5	1919	DB
E8C6	1843	IRET	E8C6	1920	DB
E8C7	1844	IRET	E8C7	1921	DB
E8C8	1845	IRET	E8C8	1922	DB
E8C9	1846	IRET	E8C9	1923	DB
E8CA	1847	IRET	E8CA	1924	DB
E8CB	1848	IRET	E8CB	1925	DB
E8CC	1849	IRET	E8CC	1926	DB
E8CD	1850	IRET	E8CD	1927	DB
E8CE	1851	IRET	E8CE	1928	DB
E8CF	1852	IRET	E8CF	1929	DB
E8D0	1853	IRET	E8D0	1930	DB
E8D1	1854	IRET	E8D1	1931	DB
E8D2	1855	IRET	E8D2	1932	DB
E8D3	1856	IRET	E8D3	1933	DB
E8D4	1857	IRET	E8D4	1934	DB
E8D5	1858	IRET	E8D5	1935	DB
E8D6	1859	IRET	E8D6	1936	DB
E8D7	1860	IRET	E8D7	1937	DB
E8D8	1861	IRET	E8D8	1938	DB
E8D9	1862	IRET	E8D9	1939	DB
E8DA	1863	IRET	E8DA	1940	DB
E8DB	1864	IRET	E8DB	1941	DB
E8DC	1865	IRET	E8DC	1942	DB
E8DD	1866	IRET	E8DD	1943	DB
E8DE	1867	IRET	E8DE	1944	DB
E8DF	1868	IRET	E8DF	1945	DB
E8E0	1869	IRET	E8E0	1946	DB
E8E1	1870	IRET	E8E1	1947	DB
E8E2	1871	IRET	E8E2	1948	DB
E8E3	1872	IRET	E8E3	1949	DB
E8E4	1873	IRET	E8E4	1950	DB
E8E5	1874	IRET	E8E5	1951	DB
E8E6	1875	IRET	E8E6	1952	DB
E8E7	1876	IRET	E8E7	1953	DB
E8E8	1877	IRET	E8E8	1954	DB
E8E9	1878	IRET	E8E9	1955	DB
E8EA	1879	IRET	E8EA	1956	DB
E8EB	1880	IRET	E8EB	1957	DB
E8EC	1881	IRET	E8EC	1958	DB
E8ED	1882	IRET	E8ED	1959	DB
E8EE	1883	IRET	E8EE	1960	DB
E8EF	1884	IRET	E8EF	1961	DB
E8F0	1885	IRET	E8F0	1962	DB
E8F1	1886	IRET	E8F1	1963	DB
E8F2	1887	IRET	E8F2	1964	DB
E8F3	1888	IRET	E8F3	1965	DB
E8F4	1889	IRET	E8F4	1966	DB
E8F5	1890	IRET	E8F5	1967	DB

LOC OBJ	LINE	SOURCE	LOC OBJ	LINE	SOURCE
E994 80D8	1798	MOV OS,AX	1075	MOV AX,INS_KEY+256	: SET SCAN CODE INTO AX, 0 INTO AL
E995 84D0	1799	IN AL,KB_DATA	1076	JMP K57	: PUT INTO OUTPUT BUFFER
E996 84D0	1800	PUSH AX	1077		
E997 8461	1801	IN AL,KB_CTL	1078		
E998 84E0	1802	MOV AX,AL	1079		
E999 0C60	1803	OR AL,0BH	1080		
E99F 8661	1804	OUT KB_CTL,AL	1081	CHP AM,SCROLL_SHIFT	: BREAK-SHIFT-FOUND
E9A1 86E0	1805	XOR AL,AL	1082	JAE K24	: IS THIS A TOGGLE KEY
E9A3 8661	1806	OUT KB_CTL,AL	1083	NOT AH	: YES, HANDLE BREAK TOGGLE
E9A5 58	1807	MOV AX,AX	1084	CHP KB_FLAG,AN	: INVERT MASK
E9A6 84E0	1808	MOV AX,AL	1085	CHP AL,ALT_KEY+0BH	: TURN OFF SHIFT BIT
	1809		1086	JNE K26	: IS THIS ALTERNATE SHIFT RELEASE
	1810		1087		: INTERRUPT_RETURN
E9A8 3CFF	1811	CHP AL,OFFH	1088		
E9A9 7503	1812	JNZ K16	1089		
E9AC E97802	1813	JMP K62	1090		
	1814		1091		
	1815		1092		
	1816		1093		
	1817		1094		
E9AF	1818		1095		
E9AF 2677	1819	AND AL,OFFH	1096	CHP AL,0BH	: NO-SHIFT-FOUND
E9B1 0E	1820	PUSH CS	1097	JAE K26	: TEST FOR BREAK KEY
E9B2 07	1821	POP ES	1098	TEST KB_FLAG,1,HOLD_STATE	: NOTHING FOR BREAK CHARS FROM HERE ON
E9B3 0F82E0	1822	MOV DI,OFFSET K6	1099	JZ K26	: ARE WE IN HOLD STATE
E9B4 940800	1823	MOV CX,K6L	1100	CHP AL,MAP_KEY	: BRANCH AROUND TEST IF NOT
E9B9 F2	1824	REPNE SCASB	1101	JZ K26	
E9BA AE	1825	MOV AL,AN	1102	AND KB_FLAG,1,NOT_HOLD_STATE	: CAN'T END HOLD ON MAP_LOCK
E9BB 84C4	1826	JZ K17	1103		: TURN OFF THE HOLD STATE BIT
E9BD 7403	1827	JMP K25	1104		
E9BF E0B000	1828		1105		
	1829		1106		
	1830		1107		
E9C2 0EFA3E0	1831	SUB DI,OFFSET K6+1	1108		
E9C4 2E8A58AE0	1832	MOV AH,CS:K70101	1109		
E9C8 A800	1833	TEST AL,0BH	1110		
E9CD 7554	1834	JNZ K23	1111		
	1835		1112		
	1836		1113		
E9CF 08FC10	1837	CHP AH,SCROLL_SHIFT	1114	CLI	: INTERRUPT_RETURN
E9D2 7307	1838	JAE K16	1115	MOV AL,EOI	: TURN OFF INTERRUPTS
	1839		1116	OUT 020H,AL	: END OF INTERRUPT COMMAND
	1840		1117		: SEND COMMAND TO INTERRUPT CONTROL PORT
E9D4 08261700	1841	OR KB_FLAG,AN	1118		: INTERRUPT_RETURN-NO-EOI
E9D8 E0B000	1842	JMP K26	1119	POP ES	
	1843		1120	POP DI	
	1844		1121	POP SI	
	1845		1122	POP DX	
	1846		1123	POP CX	
	1847		1124	POP BX	
E9D8	1848		1125	POP AX	
E9D8 F666170004	1849	TEST KB_FLAG,CTL_SHIFT	1126	IRET	: RESTORE STATE
E9E0 7508	1850	JNZ K25	1127		: RETURN, INTERRUPTS BACK ON WITH FLAG CHANGE
E9E2 3C52	1851	CHP AL,INS_KEY	1128		
E9E4 7325	1852	JNZ K22	1129		
E9E6 7325	1853	TEST KB_FLAG,ALT_SHIFT	1130		
E9E8 F666170008	1854	JZ K19	1131	TEST KB_FLAG,ALT_SHIFT	: NO-HOLD-STATE
E9EB 7403	1855	JMP K25	1132	JNZ K29	: ARE WE IN ALTERNATE SHIFT
E9ED E0B890	1856	TEST KB_FLAG,MAP_STATE	1133	JMP K36	: JUMP IF NOT ALTERNATE
E9F0 F666170020	1857	JNZ K21	1134		
E9F5 7500	1858	TEST KB_FLAG,LEFT_SHIFT	1135		
E9F7 F666170003	1859	JZ K22	1136		
E9FC 7400	1860		1137		
E9FE	1861		1138		
E9FE 803052	1862	MOV AX,530H	1139		
E9A1 E0B001	1863	JMP K57	1140		
E9A4	1864		1141		
E9A4 F666170003	1865	TEST KB_FLAG,LEFT_SHIFT+RIGHT_SHIFT	1142		
E9A9 74F3	1866	JZ K20	1143		
	1867		1144		
E9AB	1868		1145		
E9AB 84261800	1869	TEST AN,KB_FLAG,1	1146		
E9AF 7540	1870	JNZ K26	1147		
E9B1 08261800	1871	OR KB_FLAG,AN	1148		
E9B3 30261700	1872	XOR KB_FLAG,AN	1149		
E9B5 3C52	1873	CHP AL,INS_KEY	1150		
E9B7 7541	1874	JNE K26			

LOC OBJ	LINE	SOURCE
E801 0B01E00	R	2026
E813 0B01E00	R	2027
E817 0B01E00	R	2028
E818 0B06710000	R	2029
E820 001B		2030
E822 000000		2031
E825 0B0400		2032
E828		2033
E828 3C45		2034
E830 7521		2035
E83C 800E180000	R	2036
E831 0B02		2037
E833 0B20		2038
E833 0B20		2039
E833 0B20		2040
E835 0B0400		2041
E835 0B0400		2042
E835 0B0400		2043
E835 0B0400		2044
E835 0B0400		2045
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E835 0B0400		2067
E835 0B0400		2068
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E835 0B0400		2109
E835 0B0400		2110
E835 0B0400		2111
E835 0B0400		2112
E835 0B0400		2113
E835 0B0400		2114
E835 0B0400		2115
E835 0B0400		2116
E835 0B0400		2117
E835 0B0400		2118
E835 0B0400		2119
E835 0B0400		2120
E835 0B0400		2121
E835 0B0400		2122
E835 0B0400		2123
E835 0B0400		2124
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E835 0B0400		2126
E835 0B0400		2127
E835 0B0400		2128
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E835 0B0400		2141
E835 0B0400		2142
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E835 0B0400		2145
E835 0B0400		2146
E835 0B0400		2147
E835 0B0400		2148

LOC OBJ	LINE	SOURCE	LOC OBJ	LINE	SOURCE
EB90 E90700	2103	JMP K63	EBF1 740F	2180	JZ K66
EB93	2104	K47: ; TRANSLATE_SCAN	2181		
EB93 8B1FE9	2105	MOV BX,OFFSET K11	2182	1-----	CONVERT ANY UPPER CASE TO LOWER CASE
EB96 EB040	2107	JMP SHORT K56	2183		
	2108	1-----	2184	CMF AL,'A'	IF NOT SHIFT, CONVERT LOWER TO UPPER
	2109	KEYPAD KEYS, MUST TEST NPM LOCK FOR DETERMINATION	2185	JB K61	IF NOT CAPS STATE
	2110		2186	CMF AL,'Z'	IF NOT CAPS STATE
EB96	2111	K48: ; KEYPAD-REGION	2187	JA K61	IF NOT CAPS STATE
EB96 6A6170020	2112	TEST KB_FLAG-NPM_STATE	2188	ADD AL,'A'-'A'	CONVERT TO LOWER CASE
EB9D 7520	2113	JNZ K52	2189	JMP SHORT K61	IF NOT CAPS STATE
EB9F 6A6170003	2114	TEST KB_FLAG-LEFT_SHIFT+RIGHT_SHIFT	2190		
EBAA 7520	2115	JNZ K53	2191	K59: ; NEAR-INTERLUPT-RETURN	
	2116	1-----	2192	JMP K26	IF INTERRUPT_RETURN
	2117	BASE CASE FOR KEYPAD	2193	1-----	CONVERT ANY LOWER CASE TO UPPER CASE
	2118		2194		
EBAA	2119	K49: ; BASE-CASE	2195		
EBAA 5CA4	2120	CMF AL,'A'	2196	CMF AL,'A'	LOWER-TO-UPPER
EBAA 740D	2121	JE K50	2197	JB K61	IF NOT CAPS STATE
EBAA 5CAE	2122	CMF AL,'Z'	2198	CMF AL,'Z'	IF NOT CAPS STATE
EBAC 740E	2123	CMF AL,'Z'	2199	JA K61	IF NOT CAPS STATE
EBAC 5CA5	2124	JE K51	2200	SUB AL,'A'-'A'	CONVERT TO UPPER CASE
EBAC 5CA5	2125	SUB AL,'A'-'A'	2201		
EBB0 8B7AE9	2126	MOV BX,OFFSET K15	2202	K61: ; NOT-CAPS-STATE	
EBB3 EB77	2127	JMP SHORT K64	2203	MOV BX,BUFFER_TAIL	GET THE END POINTER TO THE BUFFER
EBB5 8B204A	2128	MOV AX,744256+1	2204	MOV SI,BX	SAVE THE VALUE
EBB8 EB22	2129	JMP SHORT K57	2205	CALL K4	ADVANCE THE TAIL
EBBA 8B284E	2130	MOV AX,744256+1	2206	CMF BX,BUFFER_HEAD	HAS THE BUFFER WRAPPED AROUND
EBBA EB10	2131	JMP SHORT K57	2207	JE K62	IF NOT CAPS STATE
	2132	1-----	2208	MOV SI,1,AX	STORE THE VALUE
	2133	NIGHT BE NPM LOCK, TEST SHIFT STATUS	2209	MOV BX,BUFFER_TAIL+BX	MOVE THE POINTER UP
	2134		2210	JMP K26	IF INTERRUPT_RETURN
	2135		2211		
	2136	K52: ; ALMOST-NPM-STATE	2212	1-----	BUFFER IS FULL, SOUND THE BEEPER
EBBF	2137	TEST KB_FLAG-LEFT_SHIFT+RIGHT_SHIFT	2213		
EBBF 6A6170003	2138	JNZ K49	2214		
EBCA 7520	2139	1-----	2215	CALL ERROR_BEEP	IF BUFFER-FULL-BEEP
EBCC	2140		2216	JMP K26	IF INTERRUPT_RETURN
EBCC 5C46	2141	SUB AL,'A'	2217		
EBCC 5C46	2142	MOV BX,OFFSET K14	2218	1-----	TRANSLATE_SCAN FOR PSEUDO_SCAN CODES
EBCC 8B0D09	2143	CMF AL,'Z'	2219		
EBCC EB08	2144	JMP SHORT K56	2220	K63: ; TRANSLATE-SCAN	
	2145	1-----	2221	SUB AL,'A'	CONVERT ORIGIN TO FUNCTION KEYS
	2146	PLAIN OLD LOWER CASE	2222	XLAT	TRANSLATE_SCAN-ORIG
EBCC	2147		2223	CMF AL,'A'	IF NOT CAPS STATE
EBCC 5C46	2148	CMF AL,'A'	2224	MOV AX,AL	IF NOT CAPS STATE
EBCC 7204	2149	JE K55	2225	MOV AX,AL	IF NOT CAPS STATE
EBD1 8B00	2150	MOV AL,0	2226	JMP K57	IF NOT CAPS STATE
EBD3 EB07	2151	JMP SHORT K57	2227		
EBD5	2152		2228	KB_INT END	
EBD5 8B05E8	2153	MOV BX,OFFSET K10	2229	PROC NEAR	SAVE REGISTERS
	2154	1-----	2230	PUSH AX	
	2155	TRANSLATE THE CHARACTER	2231	PUSH BX	
EBD8	2156		2232	PUSH CX	
EBD8 7EC8	2157	DEC AL	2233	MOV BX,0C0H	NUMBER OF CYCLES FOR 1/6 SECOND TONE
EBDA 2E07	2158	XLAT CS:K11	2234	IN AL,KB_CTL	GET CONTROL INFORMATION
	2159	1-----	2235	PUSH AX	SAVE
	2160	PUT CHARACTER INTO BUFFER	2236		
EBDC	2161		2237	K65: ; BEEP-CYCLE	
EBDC 5C46	2162	CMF AL,'A'	2238	MOV AL,0C0H	TURN OFF TONE GATE AND SPEAKER DATA
EBDC 5C46	2163	JE K59	2239	OUT KB_CTL,AL	OUTPUT TO CONTROL
EBDE 741F	2164	CMF AL,'A'	2240	MOV CX,40H	HALF CYCLE TIME FOR TONE
EBDE 4070FF	2165	CMF AL,'A'	2241	LOOP K66	SPEAKER OFF
EBE3 741A	2166	JE K59	2242	OR AL,Z	TURN ON SPEAKER BIT
	2167	1-----	2243	OUT KB_CTL,AL	OUTPUT TO CONTROL
	2168	HANDLE THE CAPS LOCK PROBLEM	2244	MOV CX,40H	SET UP COUNT
EBE5	2169		2245	LOOP K67	ANOTHER HALF CYCLE
EBE5 6A6170040	2170	TEST KB_FLAG-CAPS_STATE	2246	DEC BX	TOTAL TIME COUNT
EBEA 7420	2171	JZ K61	2247	JNZ K65	DO ANOTHER CYCLE
	2172	1-----	2248	POP AX	RECOVER CONTROL
	2173	IN CAPS LOCK STATE	2249	OUT KB_CTL,AL	OUTPUT THE CONTROL
	2174		2250	POP CX	RECOVER REGISTERS
	2175		2251	POP BX	
	2176		2252	POP AX	
	2177	1-----	2253	RET	
EBEC 6A6170003	2178	TEST KB_FLAG-LEFT_SHIFT+RIGHT_SHIFT	2254	ERROR_BEEP	END


```

LOC OBJ          LINE      SOURCE
-----
2255  I--- INT 13 -----
2256  DISKETTE 1/0
2257  : INPUT
2258  :
2259  : (AM1)0  RESET DISKETTE SYSTEM
2260  :
2261  : (AM1)1  READ THE STATUS OF THE SYSTEM INTO IAL
2262  :
2263  : (AM1)2  DISKETTE STATUS FROM LAST OPN IS USED
2264  :
2265  : REGISTERS FOR READ/WRITE/VERIFY/FORMAT
2266  :
2267  : (IM1) = DRIVE NUMBER (0-3 ALLOWED, NOT VALUE CHECKED)
2268  :
2269  : (IM1) = HEAD NUMBER (0-1 ALLOWED, NOT VALUE CHECKED)
2270  :
2271  : (IM1) = TRACK NUMBER (0-39, NOT VALUE CHECKED)
2272  :
2273  : (IM1) = SECTOR NUMBER (1-8, NOT VALUE CHECKED)
2274  :
2275  : (IM1) = NUMBER OF SECTORS ( MAX = 8, NOT VALUE CHECKED)
2276  :
2277  : (ES1)X1 = ADDRESS OF BUFFER ( NOT REQUIRED FOR VERIFY)
2278  :
2279  : (AM1)2  READ THE DESIRED SECTORS INTO MEMORY
2280  :
2281  : (AM1)3  WRITE THE DESIRED SECTORS FROM MEMORY
2282  :
2283  : (AM1)4  VERIFY THE DESIRED SECTORS
2284  :
2285  : (AM1)5  FORMAT THE DESIRED TRACK
2286  :
2287  :
2288  : FOR THE FORMAT OPERATION, THE BUFFER POINTER (ES:BX) MUST
2289  :
2290  : POINT TO THE COLLECTION OF DESIRED ADDRESS FIELDS FOR THE
2291  :
2292  : TRACK. EACH FIELD IS COMPOSED OF 4 BYTES, (C,H,P,N), WHERE
2293  :
2294  : C = TRACK NUMBER, H=HEAD NUMBER, R = SECTOR NUMBER, N= NUMBER
2295  :
2296  : OF BITES PER SECTOR (0-128, 01-256, 02-512, 03-1024)
2297  :
2298  : THERE MUST BE ONE ENTRY FOR EVERY SECTOR ON THE TRACK.
2299  :
2300  : THIS INFORMATION IS USED TO FIND THE REQUESTED SECTOR DURING
2301  :
2302  : READ/WRITE ACCESS.
2303  :
2304  : DATA VARIABLE --- DISK POINTER
2305  :
2306  : DOUBLE WORD POINTER TO THE CURRENT SET OF DISKETTE PARAMETERS
2307  :
2308  : OUTPUT
2309  :
2310  : AN = STATUS OF OPERATION
2311  :
2312  : STATUS BITS ARE DEFINED IN THE EQUATES FOR DISKETTE_STATUS
2313  :
2314  : VARIABLE IN THE DATA SEGMENT OF THIS MODULE
2315  :
2316  : CY = 0  SUCCESSFUL OPERATION (AM:0 ON RETURN)
2317  :
2318  : CY = 1  FAILED OPERATION (AM HAS ERROR REASON)
2319  :
2320  : FOR READ/WRITE/VERIFY
2321  :
2322  : OS:BX:DX:CH:CL PRESERVED
2323  :
2324  : AL = NUMBER OF SECTORS ACTUALLY READ
2325  :
2326  : ***** AL MAY NOT BE CORRECT IF THE OUT ERROR OCCURS
2327  :
2328  : NOTE: IF AN ERROR IS REPORTED BY THE DISKETTE CODE, THE APPROPRIATE
2329  :
2330  : ACTION IS TO RESET THE DISKETTE, THEN REPEAT THE OPERATION.
2331  :
2332  : ON READ ACCESS, NO MOTOR START DELAY IS TAKEN, SO THAT
2333  :
2334  : THREE RETRIES ARE REQUIRED ON HEADS TO ENSURE THAT THE
2335  :
2336  : PROBLEM IS NOT DUE TO MOTOR START-UP.
2337  :
2338  : -----
2339  : ASSUME CS:CODE,DS:DATA,ES:DATA
2340  :
2341  : DISKETTE_IO  PROC  FAR
2342  :
2343  : STI
2344  :
2345  : PUSH  BX
2346  :
2347  : PUSH  CX
2348  :
2349  : PUSH  DX
2350  :
2351  : PUSH  SI
2352  :
2353  : PUSH  DI
2354  :
2355  : PUSH  BP
2356  :
2357  : PUSH  OK
2358  :
2359  : MOV  BP,SP
2360  :
2361  : MOV  SI,DATA
2362  :
2363  : CALL  J1
2364  :
2365  : MOV  BX,4
2366  :
2367  : CALL  GET_PARM
2368  :
2369  : MOV  MOTOR_COUNT,AX
2370  :
2371  : MOV  AM,DISKETTE_STATUS
2372  :
2373  : CHP  AM,1
2374  :
2375  : CHC
2376  :
2377  : POP  DX
2378  :
2379  : POP  BP
2380  :
2381  : POP  SI
2382  :
2383  : POP  DI
2384  :
2385  : POP  CX
2386  :
2387  : POP  BX
2388  :
2389  : RET  2
2390  :
2391  : DISKETTE_IO  ENDP
2392  :
2393  : J1  PROC
2394  :
2395  :
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LOC OBJ	LINE	SOURCE	LOC OBJ	LINE	SOURCE
	2497	DISKETTE READ		2494	POP DX ; RECOVER REGISTERS
	2498			2495	----- WAIT FOR MOTOR IF WRITE OPERATION
ED0E 0044	2499	DISK_READ PROC NEAR	ED0E 5A	2496	
ED10	2500	MOV AL,040H ; DISK READ CONT		2497	TEST MOTOR_STATUS,B0H ; IS THIS A WRITE
ED10 E0B901	2501	J9: CALL DDA,SETUP ; SET UP THE DDA	ED0A 7412	2508	JZ J16 ; NO, CONTINUE WITHOUT WAIT
ED13 0446	2502	MOV AH,040H ; SET UP THE OPERATION	ED0A B01600	2509	MOV BX,20 ; GET THE MOTOR WAIT
ED15 E036	2503	DISK_READ PROC NEAR	ED00 E0E000	2509	CALL GET_PARM ; PARAMETER
	2504		ED00 04E4	2509	OR AH,AN ; TEST FOR NO WAIT
	2505	DISKETTE VERIFY	ED02	2509	J12: JZ J16 ; TEST WAIT TIME
ED17	2506	DISK_VERIFY PROC NEAR	ED02 7408	2509	SUB CX,CX ; EXIT WITH TIME EXPIRED
ED17 B042	2507	MOV AL,040H ; VERIFY COMMAND FOR DDA	ED04 20C9	2509	SUB CX,CX ; SET UP 1/8 SECOND LOOP TIME
ED19 E0F5	2508	J9: J9 ; DO AS IF DISK READ	ED04 E2FE	2509	LOOP J13 ; WAIT FOR THE REQUIRED TIME
	2509	DISK_VERIFY ENDP	ED08 FECC	2509	DEC AH ; DECREMENT THE VALUE
	2510	DISKETTE FORMAT	ED0A E0F6	2509	JMP J12 ; ARE WE DONE YET
	2511	DISKETTE WRITE ROUTINE	ED0C	2509	J14: STI ; MOTOR RUNNING
ED1B	2512	DISK_FORMAT PROC NEAR	ED0C FB	2509	POP CX ; INTERRUPTS BACK ON FOR BIPASS WAIT
ED1B 0003F0000	2513	OR MOTOR_STATUS,B0H ; INDICATE WRITE OPERATION	ED00 59	2509	----- DO THE SEEK OPERATION
ED20 B04A	2514	MOV AL,040H ; WILL WRITE TO THE DISKETTE		2509	CALL SEEK ; MOVE TO CORRECT TRACK
ED22 E0A701	2515	CALL DDA,SETUP ; SET UP THE DDA	ED01 58	2509	MOV AX ; RECOVER COMMAND
ED23 B040	2516	MOV AH,040H ; ESTABLISH THE FORMAT COMMAND	ED02 04FC	2509	MOV BH,AN ; SAVE COMMAND IN BH
ED27 E024	2517	JMP SHORT BH,OPN ; DO THE OPERATION	ED04 B600	2509	MOV DH,0 ; SET NO SECTORS READ IN CASE OF ERROR
ED29	2518	J10: MOV BX,7 ; CONTINUATION OF RH,OPN FOR FMT	ED04 7248	2510	JC J17 ; IF ERROR, THEN EXIT AFTER MOTOR OFF
ED29 B00700	2519	CALL GET_PARM ; GET THE	ED04 REF3099	2511	MOV SI,OFFSET J17 ; DUPLY RETURN ON STACK FOR NEC OUTPUT
ED2C E04101	2520	MOV BX,9 ; BYTES/SECTOR VALUE TO NEC	ED04 56	2512	PUSH SI ; SO THAT IT WILL RETURN TO MOTOR OFF LOCATION
ED2E E03001	2521	CALL GET_PARM ; GET THE		2513	----- SEND OUT THE PARAMETERS TO THE CONTROLLER
ED32 B00700	2522	MOV BX,15 ; SECTORS/TRACK VALUE TO NEC	ED00 E0A000	2514	CALL NEC_OUTPUT ; OUTPUT THE OPERATION COMMAND
ED35 E03001	2523	CALL GET_PARM ; GET THE	ED00 A4A001	2515	MOV AH,IBP+1 ; GET THE CURRENT HEAD NUMBER
ED38 E03001	2524	CALL GET_PARM ; GET THE	ED03 00E4	2516	SAL AH,1 ; MOVE IT TO BIT 2
ED3B B0100	2525	MOV BX,17 ; GAP LENGTH VALUE TO NEC	ED05 00E4	2517	SAL AH,1 ; ISOLATE THAT BIT
ED3B B0100	2526	MOV BX,17 ; GET THE FILLER BYTE	ED07 B0E404	2518	MOV AH,4 ; ON IN THE DRIVE NUMBER
ED3E E0A000	2527	JMP J16 ; TO THE CONTROLLER	ED0A 04E2	2519	OR AH,DL ; CALL NEC_OUTPUT
	2528	DISK_WRITE ENDP	ED0C E0E500	2520	CALL NEC_OUTPUT ; TEST FOR FORMAT COMMAND
	2529	DISK_WRITE PROC NEAR		2521	----- TEST FOR FORMAT COMMAND
ED41	2530	DISK_WRITE PROC NEAR	ED0F B0F740	2522	CHP BH,040H ; IS THIS A FORMAT OPERATION
ED41 0003F0000	2531	OR MOTOR_STATUS,B0H ; INDICATE WRITE OPERATION	ED02 7503	2523	JNE J15 ; NO, CONTINUE WITH R/W
ED44 B04A	2532	MOV AL,040H ; DDA WRITE COMMAND	ED04 E0A2FF	2524	JMP J10 ; IF SO, HANDLE SPECIAL
ED48 E08101	2533	MOV AH,050H ; NEC COMMAND TO WRITE TO DISKETTE		2525	----- LET THE OPERATION HAPPEN
ED48 B445	2534	DISK_WRITE ENDP	ED07 A0E5	2526	MOV AH,CH ; CYLINDER NUMBER
	2535	THIS ROUTINE PERFORMS THE READ/WRITE/VERIFY OPERATION	ED09 E07000	2527	CALL NEC_OUTPUT ; HEAD NUMBER FROM STACK
ED40	2536	RH,OPN PROC NEAR	ED0C A4A001	2528	MOV AH,IBP+1 ; HEAD NUMBER FROM STACK
ED40 7308	2537	JNC J11 ; TEST FOR DDA ERROR	ED0F E07200	2529	CALL NEC_OUTPUT ; SECTOR NUMBER
ED4F C004410009	2538	MOV DISKETTE_STATUS,DDA_BOUNDARY ; SET ERROR	ED02 A4E1	2530	CALL NEC_OUTPUT ; BYTES/SECTOR PARM FROM BLOCK
ED54 B000	2539	MOV AL,0 ; NO SECTORS TRANSFERRED	ED04 E0A000	2531	MOV BX,7 ; TO THE NEC
ED56 C3	2540	RET ; RETURN TO MAIN ROUTINE	ED07 B00700	2532	CALL GET_PARM ; EOT PARM FROM BLOCK
ED57	2541	J11: MOV AL,OPN ; SHIFT THE MASK BIT	ED0A E09100	2533	CALL GET_PARM ; TO THE NEC
ED57 50	2542	PUSH AX ; SAVE THE COMMAND	ED00 B00900	2534	MOV BX,9 ; GAP LENGTH PARM FROM BLOCK
	2543	----- TURN ON THE MOTOR AND SELECT THE DRIVE	ED03 B00800	2535	MOV BX,11 ; TO THE NEC
ED58 51	2544	PUSH CX ; SAVE THE T/S PARMS	ED0A E0A000	2536	CALL GET_PARM ; DTL PARM FROM BLOCK
ED59 A0CA	2545	MOV CL,DL ; GET DRIVE NUMBER AS SHIFT COUNT	ED03 B00900	2537	MOV BX,13 ; TO THE NEC
ED5B 0001	2546	MOV AL,1 ; MASK FOR DETERMINING MOTOR BIT	ED0A E0A000	2538	CALL GET_PARM ; RLOPN FINISH
ED5D 02E0	2547	SAL AL,CL ; SHIFT THE MASK BIT	ED0C E0A000	2539	CALL GET_PARM ; CAN NOW DISCARD THAT DUMMY RETURN ADDRESS
ED5F FA	2548	CLI ; NO INTERRUPTS WHILE DETERMINING MOTOR STATUS		2540	----- LET THE OPERATION HAPPEN
ED60 C0044000FF	2549	MOV MOTOR_COUNT,OFFN ; SET LARGE COUNT DURING OPERATION	ED0F E04001	2541	CALL WAIT_INT ; WAIT FOR THE INTERRUPT
ED65 04043F00	2550	TEST AL,MOTOR_STATUS ; TEST THAT MOTOR FOR OPERATING	ED03	2542	JZ J21 ; MOTOR OFF
ED69 7531	2551	JNZ J14 ; IF RUNNING, SKIP THE WAIT	ED03 7245	2543	JC J21 ; LOOK FOR ERROR
ED6B 00263F00F0	2552	AND MOTOR_STATUS,OPN ; TURN OFF ALL MOTOR BITS	ED0F E07301	2544	CALL RESULTS ; GET THE NEC STATUS
ED70 B0043F00	2553	OR MOTOR_STATUS,AL ; TURN ON THE CURRENT MOTOR	ED0F 723F	2545	JC J20 ; LOOK FOR ERROR
ED74 F8	2554	STI ; INTERRUPTS BACK ON		2546	----- CHECK THE RESULTS RETURNED BY THE CONTROLLER
ED75 B010	2555	MOV AL,10H ; MASK BIT	ED0A FC	2547	CLO ; SET THE CORRECT DIRECTION
ED77 02E0	2556	SAL AL,CL ; DEVELOP BIT MASK FOR MOTOR ENABLE	ED0F B04200	2548	MOV SI,OFFSET NEC_STATUS ; POINT TO STATUS FIELD
ED79 0AC2	2557	OR AL,DL ; GET DRIVE SELECT BITS IN	ED0E AC	2549	LODS NEC_STATUS ; GET STO
ED7B 00C0	2558	OR AL,0CH ; NO RESET, ENABLE DDA/INT	ED0F 24C0	2550	AND AL,0C0H ; TEST FOR NORMAL TERMINATION
ED7D 52	2559	PUSH DX ; SAVE REG			
ED7E B0F203	2560	MOV DX,0F20H ; CONTROL PORT ADDRESS			
ED81 EE	2561	OUT DX,AL			

LOC OBJ	LINE	SOURCE	LOC OBJ	LINE	SOURCE
EE01 743B	2561	JZ J22	EE52 000E10080	2639	R
EE03 3C40	2562	CHP AL:Q40H	EE57 59	2640	POP CX
EE05 7529	2563	JNZ J18	EE58 5A	2641	POP DX
	2564	;	EE59 5B	2642	POP AX
	2565	;	EE5A F9	2643	STC
	2566	;	EE5B C3	2644	RET
EE07 AC	2567	LDOS NEC_STATUS	EE5C	2645	J25:
EE08 D0E0	2568	SAL AL:1	EE5C 33C9	2646	XOR CX,CX
EE0A B404	2569	MOV AN:RECORD_NOT_FND	EE5E	2647	J26:
EE0C 7224	2570	JC J19	EE5E EC	2648	IN AL,DX
EE0E D0E0	2571	SAL AL:1	EE5F A800	2649	TEST AL,080H
EE10 D0E0	2572	SAL AL:1	EE61 7504	2650	JNZ J27
EE12 721C	2573	MOV AN:BAD_CRC	EE61 7504	2651	JNZ J27
EE14 B400	2574	JC J19	EE63 E2F9	2652	LDOR J26
EE16 D0E0	2575	SAL AL:1	EE65 E2F9	2653	JMP J26
EE18 B400	2576	MOV AN:BAD_OPM	EE67	2654	J27:
EE1A 7216	2577	JC J19	EE67 84C4	2655	MOV AL,AX
EE1C D0E0	2578	SAL AL:1	EE69 BA503	2656	MOV DX,03F5H
EE1E D0E0	2579	SAL AL:1	EE6C 1E	2657	OUT DX,AL
EE20 B404	2580	MOV AN:RECORD_NOT_FND	EE6D 59	2658	POP CX
EE22 720E	2581	JC J19	EE6E 5A	2659	POP DX
EE24 D0E0	2582	SAL AL:1	EE6F C3	2660	RET
EE26 B403	2583	MOV AN:WRITE_PROTECT		2661	NEC_OUTPUT
EE28 7209	2584	JC J19		2662	;
EE2A D0E0	2585	SAL AL:1		2663	;
EE2C B402	2586	MOV AN:BAD_ADDR_MARK		2664	;
EE2E 7202	2587	JC J19		2665	;
	2588	;		2666	;
	2589	;		2667	;
EE30 B420	2590	J18: MOV AN:BAD_NEC		2668	;
EE32	2591	J19: OR DISKETTE_STATUS,AX		2669	;
EE34 002A4100	2592	CALL NUM_TRANS		2670	;
EE36 E07701	2593	CALL NUM_TRANS		2671	;
EE38	2594	J20: RET		2672	;
EE39 C3	2595	J21: CALL RESULTS		2673	;
	2596	RET		2674	;
	2597	;		2675	;
	2598	;		2676	;
EE3A	2599	J22: CALL NUM_TRANS		2677	;
EE3C E06701	2600	XOR AN,AX		2678	;
EE41 32C4	2601	RET		2679	;
EE43 C3	2602	;		2680	;
	2603	;		2681	;
	2604	;		2682	;
EE4E	2605	J22: CALL NUM_TRANS		2683	;
EE4F E06701	2606	XOR AN,AX		2684	;
EE51 32C4	2607	RET		2685	;
EE53 C3	2608	;		2686	;
	2609	;		2687	;
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	2611	;		2689	;
	2612	;		2690	;
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	2621	;		2699	;
	2622	;		2700	;
	2623	;		2701	;
	2624	;		2702	;
	2625	;		2703	;
	2626	;		2704	;
	2627	;		2705	;
	2628	;		2706	;
	2629	;		2707	;
	2630	;		2708	;
	2631	;		2709	;
	2632	;		2710	;
	2633	;		2711	;
	2634	;		2712	;
	2635	;		2713	;
	2636	;		2714	;
	2637	;		2715	;
	2638	;			

LOC	OBJ	LINE	SOURCE
EF02 E605	2793		OUT DMA+5,AL ; LOW BYTE OF COUNT
EF04 8AC4	2794		MOV AL,AM ; HIGH BYTE OF COUNT
EF06 E605	2795		OUT DMA+5,AL ; RECOVER COUNT VALUE
EF08 59	2796		POP CX ; ADD, TEST FOR 64K OVERFLOW
EF09 58	2797		ADD AX,CX ; RECOVER REGISTER
EF0A 03C1	2798		ADD AX,CX ; RECOVER REGISTER
EF0C 59	2799		POP CX ; RECOVER REGISTER
EF0D 0002	2800		MOV AL,Z ; MODE FOR 8:37
EF0F E60A	2801		OUT DMA+10,AL ; INITIALIZE THE DISKETTE CHANNEL
EF11 C3	2802		RET ; RETURN TO CALLER, CPL SET BY ABOVE IF ERROR
EF12 E81E00	2803		DMA_SETUP ENDP
EF15 7214	2804		CALL WAIT_INT ; WAIT FOR THE INTERRUPT
EF17 8408	2805		MOV AH,08H ; IF ERROR, RETURN IT
EF19 E820FF	2806		CALL INEC_OUTPUT ; SENSE INTERRUPT STATUS COMMAND
EF1C E8AC00	2807		CALL RESULTS ; READ IN THE RESULTS
EF1F 722A	2808		MOV AL,HEC_STATUS ; GET THE FIRST STATUS BYTE
EF21 A0C200	2809		AND AL,060H ; ISOLATE THE BITS
EF24 2460	2810		MOV AL,060H ; TEST FOR CORRECT VALUE
EF26 3C60	2811		CMPL AL,060H ; IF ERROR, GO MARK IT
EF28 7402	2812		JZ J35 ; GOOD RETURN
EF2A F8	2813		CLC ; RETURN TO CALLER
EF2B	2814		RET ; CMK2_ERROR
EF2C C3	2815		J35: OR DISKETTE_STATUS,0A0_SEEK ; ERROR RETURN CODE
EF2E 80E410040	2816		STC ; WAIT_INT
EF31 F9	2817		RET ; CMK_STAT_2 ENDP
EF32 C3	2818		CMK_STAT_2 ENDP
EF33	2819		WAIT_INT ; THIS ROUTINE WAITS FOR AN INTERRUPT TO OCCUR
EF34	2820		THIS ROUTINE WAITS FOR AN INTERRUPT TO OCCUR
EF35	2821		A TIME OUT ROUTINE TAKES PLACE DURING THE WAIT, SO
EF36	2822		THAT AN ERROR MAY BE RETURNED IF THE DRIVE IS NOT READY
EF37	2823		INPUT ; INPUT
EF38	2824		ONE ; ONE
EF39	2825		OUTPUT ; OUTPUT
EF3A	2826		CT = 0 SUCCESS ; CT = 0 SUCCESS
EF3B	2827		CT = 1 FAILURE -- DISKETTE_STATUS IS SET ACCORDINGLY
EF3C	2828		(AX) DESTROYED ; (AX) DESTROYED
EF3D	2829		WAIT_INT PROC NEAR ; TURN ON INTERRUPTS, JUST IN CASE
EF3E	2830		STI ; SAVE REGISTERS
EF3F	2831		PUSH BX ; SAVE REGISTERS
EF40	2832		PUSH CX ; CLEAR THE COUNTERS
EF41	2833		MOV BL,2 ; SECOND LEVEL COUNTER
EF42	2834		XOR CX,CX ; FPD 2 SECOND WAIT
EF43	2835		J36: TEST SEEK_STATUS,INT_FLAG ; TEST FOR INTERRUPT OCCURRING
EF44	2836		J37: J37 ; COUNT DOWN WHILE WAITING
EF45	2837		LOOP J36 ; SECOND LEVEL COUNTER
EF46	2838		DEC BL ; DISKETTE_STATUS,TIME_OUT ; NOTHING HAPPENED
EF47	2839		J36: OR DISKETTE_STATUS,TIME_OUT ; ERROR RETURN
EF48	2840		STC ; SAVE CURRENT CARRY
EF49	2841		PUSHF ; TURN OFF INTERRUPT FLAG
EF4A	2842		AND SEEK_STATUS,NOT INT_FLAG ; RECOVER CARRY
EF4B	2843		POPDI ; RECOVER REGISTERS
EF4C	2844		POP CX ; GOOD RETURN CODE COMES FROM TEST, NOT
EF4D	2845		POP BX ;
EF4E	2846		RET ;
EF4F	2847		ENDP ;
EF50	2848		WAIT_INT ENDP
EF51	2849		
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EF53	2851		
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EF56	2854		
EF57	2855		
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EF5A	2858		
EF5B	2859		
EF5C	2860		
EF5D	2861		
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EF64	2868		
EF65	2869		

LOC OBJ	LINE	SOURCE	LOC OBJ	LINE	SOURCE
EF57	2870	DISK_INT	EF5E	2894	J43: LOOP J43
EF57 IB	2871	: DISK_INT	EF5F	2895	RESULT OPERATION IS DONE
EF58 10	2872	: THIS ROUTINE HANDLES THE DISKETTE INTERRUPT	EF60 4A	2896	J44: POP BX
EF59 50	2873	: INOUT	EF61 EC	2897	POP DX
EF5A B0A4000	2874	: NONE	EF62 A810	2898	IN AL,DX
EF5D B0D0	2875	: OUTPUT	EF63 4A10	2899	TEST AL,010H
EF5F B0D0C0000	2876	: THE INTERRUPT FLAG IS SET IS SEEK_STATUS	EF64 7A06	2900	JZ J44
EF64 B0D0	2877	: END OF INTERRUPT MARKER	EF65 F0C0	2901	DEC INCREMENT THE STATUS COUNTER
EF66 E620	2878	: INTERRUPT CONTROL PORT	EF66 75CA	2902	JNZ J38
EF68 50	2879	: RECOVER SYSTEM	EF6A E0E5	2903	JMP J41
EF69 1F	2880	: RETURN FROM INTERRUPT			
EF6A CF	2881	: RE ENABLE INTERRUPTS			
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LOC OBJ	LINE	SOURCE
	3007	1--- INT 17 -----
	3008	PRINT_IO
	3009	THIS ROUTINE PROVIDES COMMUNICATION WITH THE PRINTER
	3010	(AH)=0 PRINT THE CHARACTER IN (AL)
	3011	ON RETURN, AH=1 IF CHARACTER COULD NOT BE PRINTED (TIME OUT)
	3012	OTHER BITS SET AS ON NORMAL STATUS CALL
	3013	INITIALIZE THE PRINTER PORT
	3014	SETUP WITH (AH) SET WITH PRINTER STATUS
	3015	(AH)=2 READ THE PRINTER STATUS INTO (AH)
	3016	7 6 5 4 3 2-1 0
	3017	1 = BUSY
	3018	1 = ACKNOWLEDGE
	3019	1 = OUT OF PAPER
	3020	1 = SELECTED
	3021	1 = 1/0 ERROR
	3022	UNUSED
	3023	1 = BUSY
	3024	1 = ACKNOWLEDGE
	3025	1 = OUT OF PAPER
	3026	1 = SELECTED
	3027	1 = 1/0 ERROR
	3028	UNUSED
	3029	1 = BUSY
	3030	1 = ACKNOWLEDGE
	3031	1 = OUT OF PAPER
	3032	1 = SELECTED
	3033	1 = 1/0 ERROR
	3034	UNUSED
	3035	1 = BUSY
	3036	1 = ACKNOWLEDGE
	3037	1 = OUT OF PAPER
	3038	1 = SELECTED
	3039	1 = 1/0 ERROR
	3040	UNUSED
	3041	1 = BUSY
	3042	1 = ACKNOWLEDGE
	3043	1 = OUT OF PAPER
	3044	1 = SELECTED
	3045	1 = 1/0 ERROR
	3046	UNUSED
	3047	1 = BUSY
	3048	1 = ACKNOWLEDGE
	3049	1 = OUT OF PAPER
	3050	1 = SELECTED
	3051	1 = 1/0 ERROR
	3052	UNUSED
	3053	1 = BUSY
	3054	1 = ACKNOWLEDGE
	3055	1 = OUT OF PAPER
	3056	1 = SELECTED
	3057	1 = 1/0 ERROR
	3058	UNUSED
	3059	1 = BUSY
	3060	1 = ACKNOWLEDGE
	3061	1 = OUT OF PAPER
	3062	1 = SELECTED
	3063	1 = 1/0 ERROR
	3064	UNUSED
	3065	1 = BUSY
	3066	1 = ACKNOWLEDGE
	3067	1 = OUT OF PAPER
	3068	1 = SELECTED
	3069	1 = 1/0 ERROR
	3070	UNUSED
	3071	1 = BUSY
	3072	1 = ACKNOWLEDGE
	3073	1 = OUT OF PAPER
	3074	1 = SELECTED
	3075	1 = 1/0 ERROR
	3076	UNUSED
	3077	1 = BUSY
	3078	1 = ACKNOWLEDGE
	3079	1 = OUT OF PAPER
	3080	1 = SELECTED
	3081	1 = 1/0 ERROR
	3082	UNUSED
	3083	1 = BUSY
	3084	1 = ACKNOWLEDGE
	3085	1 = OUT OF PAPER
	3086	1 = SELECTED
	3087	1 = 1/0 ERROR
	3088	UNUSED
	3089	1 = BUSY
	3090	1 = ACKNOWLEDGE
	3091	1 = OUT OF PAPER
	3092	1 = SELECTED
	3093	1 = 1/0 ERROR
	3094	UNUSED
	3095	1 = BUSY
	3096	1 = ACKNOWLEDGE
	3097	1 = OUT OF PAPER
	3098	1 = SELECTED
	3099	1 = 1/0 ERROR
	3100	UNUSED
	3101	1 = BUSY
	3102	1 = ACKNOWLEDGE
	3103	1 = OUT OF PAPER
	3104	1 = SELECTED
	3105	1 = 1/0 ERROR
	3106	UNUSED
	3107	1 = BUSY
	3108	1 = ACKNOWLEDGE
	3109	1 = OUT OF PAPER
	3110	1 = SELECTED
	3111	1 = 1/0 ERROR
	3112	UNUSED
	3113	1 = BUSY
	3114	1 = ACKNOWLEDGE
	3115	1 = OUT OF PAPER
	3116	1 = SELECTED
	3117	1 = 1/0 ERROR
	3118	UNUSED
	3119	1 = BUSY
	3120	1 = ACKNOWLEDGE
	3121	1 = OUT OF PAPER
	3122	1 = SELECTED
	3123	1 = 1/0 ERROR
	3124	UNUSED
	3125	1 = BUSY
	3126	1 = ACKNOWLEDGE
	3127	1 = OUT OF PAPER
	3128	1 = SELECTED
	3129	1 = 1/0 ERROR
	3130	UNUSED
	3131	1 = BUSY
	3132	1 = ACKNOWLEDGE
	3133	1 = OUT OF PAPER
	3134	1 = SELECTED
	3135	1 = 1/0 ERROR
	3136	UNUSED
	3137	1 = BUSY
	3138	1 = ACKNOWLEDGE
	3139	1 = OUT OF PAPER
	3140	1 = SELECTED
	3141	1 = 1/0 ERROR
	3142	UNUSED
	3143	1 = BUSY
	3144	1 = ACKNOWLEDGE
	3145	1 = OUT OF PAPER
	3146	1 = SELECTED
	3147	1 = 1/0 ERROR
	3148	UNUSED
	3149	1 = BUSY
	3150	1 = ACKNOWLEDGE
	3151	1 = OUT OF PAPER
	3152	1 = SELECTED
	3153	1 = 1/0 ERROR
	3154	UNUSED
	3155	1 = BUSY
	3156	1 = ACKNOWLEDGE

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LOC OBJ      LINE      SOURCE
1 1AH156 SCROLL ACTIVE PAGE UP
2 (AL) = NUMBER OF LINES, INPUT LINES BLANKED AT BOTTOM OF WINDOW
3 (CH-CL) = ROW/COLUMN OF UPPER LEFT CORNER OF SCROLL
4 (CH-OL) = ROW/COLUMN OF LOWER RIGHT CORNER OF SCROLL
5 (BH) = ATTRIBUTE TO BE USED ON BLANK LINE
6 1AH157 SCROLL ACTIVE PAGE DOWN
7 (AL) = NUMBER OF LINES, INPUT LINES BLANKED AT TOP OF WINDOW
8 (CH-CL) = ROW/COLUMN OF UPPER LEFT CORNER OF SCROLL
9 (CH-OL) = ROW/COLUMN OF LOWER RIGHT CORNER OF SCROLL
10 (BH) = ATTRIBUTE TO BE USED ON BLANK LINE
11 CHARACTER HANDLING ROUTINES
12 1AH158 READ ATTRIBUTE/CHARACTER AT CURRENT CURSOR POSITION
13 (BH) = DISPLAY PAGE (VALID FOR ALPHA MODES ONLY)
14 ON EXIT:
15 (AL) = CHAR READ
16 (AH) = 9 WRITE ATTRIBUTE/CHARACTER AT CURRENT CURSOR POSITION
17 (BH) = DISPLAY PAGE (VALID FOR ALPHA MODES ONLY)
18 (CX) = COUNT OF CHARACTERS TO WRITE
19 (AL) = CHAR TO WRITE
20 SEE NOTE ON WRITE DOT FOR BIT 7 OF BL = 1.
21 (BH) = DISPLAY PAGE (VALID FOR ALPHA MODES ONLY)
22 (CX) = COUNT OF CHARACTERS TO WRITE
23 (AL) = CHAR TO WRITE
24 FOR READ/WRITE CHARACTER INTERFACE WHILE IN GRAPHICS MODE, THE
25 CHARACTERS ARE FORMED FROM A CHARACTER GENERATOR IMAGE
26 MAINTAINED IN THE SYSTEM ROM. ONLY THE 128 CHARS
27 ARE CONTAINED THERE. TO READ/WRITE THE SECOND 128 CHARS,
28 THE USER MUST INITIALIZE THE POINTER AT INTERRUPT 1FH
29 (LOCATION 0007CH) TO POINT TO THE 1K BYTE TABLE CONTAINING
30 THE CODE POINTS FOR THE SECOND 128 CHARS (128-255).
31 FOR WRITE CHARACTER INTERFACE IN GRAPHICS MODE, THE REPLICATION FACTOR
32 CONTAINED IN (CX) ON ENTRY WILL PRODUCE VALID RESULTS ONLY
33 FOR CHARACTERS CONTAINED ON THE SAME ROM. CONTINUATION TO
34 SUCCEEDING LINES WILL NOT PRODUCE CORRECTLY.
35 GRAPHICS INTERFACE
36 1AH159 SET COLOR PALETTE
37 (BH) = PALETTE COLOR ID BEING SET (0-127)
38 (BL) = COLOR VALUE TO BE USED WITH THAT COLOR ID
39 NOTE: FOR THE CURRENT COLOR CARD, THIS ENTRY POINT HAS
40 MEANING ONLY FOR 320x200 GRAPHICS.
41 COLOR ID = 0 SELECTS THE BACKGROUND COLOR (0-15)
42 COLOR ID = 1 SELECTS THE PALETTE TO BE USED:
43 0 = GREEN(1)/RED(2)/YELLOW(3)
44 1 = CYAN(11)/MAGENTA(12)/WHITE(13)
45 IN 40x25 OR 80x25 ALPHA MODES, THE VALUE SET FOR
46 PALETTE COLOR 0 INDICATES THE BORDER COLOR
47 TO BE USED (VALUES 0-31, WHERE 16-31 SELECT THE
48 HIGH INTENSITY BACKGROUND SET.
49 1AH160 WRITE DOT
50 (CX) = ROW NUMBER
51 (CX) = COLUMN NUMBER
52 (AL) = COLOR VALUE
53 IF BIT 7 OF AL = 1, THEN THE COLOR VALUE IS EXCLUSIVE
54 OR'D WITH THE CURRENT CONTENTS OF THE DOT
55 1AH161 READ DOT
56 (CX) = ROW NUMBER
57 (CX) = COLUMN NUMBER
58 (AL) RETURNS THE DOT READ
59 ASCII TELETYPE ROUTINE FOR OUTPUT
60 1AH162 WRITE TELETYPE
61 (AL) = CHAR TO WRITE
62 (BL) = FOREGROUND COLOR IN GRAPHICS MODE
63 (BH) = DISPLAY PAGE IN ALPHA MODE
64 NOTE -- SCREEN WIDTH IS CONTROLLED BY PREVIOUS MODE SET

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LOC OBJ      LINE      SOURCE
1 3232 (AH) = 15 CURRENT VIDEO STATE
2 RETURNS THE CURRENT VIDEO STATE
3 3233 (AL) = MODE CURRENTLY SET (SEE AH=0 FOR EXPLANATION)
4 3234 (AH) = NUMBER OF CHARACTER COLUMNS ON SCREEN
5 3235 (BH) = CURRENT ACTIVE DISPLAY PAGE
6 3236 CS-05-05-15-BX.CX-DX PRESERVED DURING CALL
7 3237 ALL OTHERS DESTROYED
8 3238 ASSUME CS:05-05-0A:ES:VIDEO_RAM
9 3239
10 3240
11 3241
12 3242
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14 3244
15 3245
16 3246
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20 3250
21 3251
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30 3260
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34 3264
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50 3280
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62 3292
63 3293
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67 3297
68 3298
69 3299
70 3300
71 3301
72 3302
73 3303
74 3304
75 3305
76 3306
77 3307

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LOC OBJ	LINE	SOURCE	LOC OBJ	LINE	SOURCE
F0A4 36A520A1F0A19	3308	DB	35H,20H,20H,0AH,1FH,6,10H	3384	F146 EE
F9A8 1CC0276607	3309	DB	1CH,2,7,6,7	3385	F147 42
F0B0 00000000	3310	DB	0,0,0,0	3386	INC AM
	3311	DB	0,0,0,0	3387	MOV AL,0X1
	3312	DB	0,0,0,0	3388	OUT DX,AL
F0B4 7150840A1F0A19	3313	DB	71H,50H,5AH,0AH,1FH,6,10H	3389	INC DX
F0B8 1CC0276607	3314	DB	1CH,2,7,6,7	3390	DEC DX
F0C0 00000000	3315	DB	0,0,0,0	3391	LOOP H10
	3316	DB	0,0,0,0	3392	POP AX
F0C4 36A520A1F0A19	3317	DB	36H,20H,20H,0AH,7FH,6,6AH	3393	POP DS
F0C8 70A2210607	3318	DB	70H,2,1,1,6,7	3394	ASSUME DS:DATA
F0D0 00000000	3319	DB	0,0,0,0	3395	
	3320	DB	0,0,0,0	3396	
F0D4 6150520F190A19	3321	DB	61H,50H,52H,0FH,1FH,6,10H	3397	
F0D8 1902000B0C	3322	DB	19H,2,00H,0BH,0CH		
F0E0 00000000	3323	DB	0,0,0,0		
	3324	DB	0,0,0,0		
F0E4 0000	3325	DB	0,0,0,0		
F0E8 0010	3326	DB	0,0,0,0		
F0F0 0040	3327	DB	0,0,0,0		
F0F4 0040	3328	DB	0,0,0,0		
	3329	DB	0,0,0,0		
	3330	DB	0,0,0,0		
	3331	DB	0,0,0,0		
F0FC	3332	DB	0,0,0,0		
F0FC 28A52050282850	3333	DB	28H,50H,50H,28H,28H,50H,28H,50H		
	3334	DB	0,0,0,0		
F0F4	3335	DB	0,0,0,0		
F0F4 2C8020240E1E29	3336	DB	2CH,20H,20H,24H,2EM,1EH,29H		
	3337	DB	0,0,0,0		
	3338	DB	0,0,0,0		
F0FC	3339	DB	0,0,0,0		
F0FC 8A0A03	3340	DB	8AH,0A03H		
F0FF 5300	3341	DB	53H,00H		
F101 83FF30	3342	DB	83H,FF30H		
F104 7507	3343	DB	75H,07H		
F106 8007	3344	DB	80H,07H		
F108 B0A0A1	3345	DB	B0H,A0A1H		
F10B FEC3	3346	DB	FBH,EC3H		
F10B 8A00	3347	DB	FBH,8A00H		
F10F 424900	3348	DB	42H,4900H		
F112 8916A300	3349	DB	89H,16A300H		
F116 1E	3350	DB	16H,1EH		
F117 50	3351	DB	17H,50H		
F118 52	3352	DB	18H,52H		
F119 83C204	3353	DB	83H,C204H		
F11C 8AC3	3354	DB	8CH,AC3H		
F11E EE	3355	DB	1EH,EEH		
F11F 5A	3356	DB	1FH,5AH		
F120 8A00	3357	DB	20H,8A00H		
F122 8E08	3358	DB	22H,8E08H		
F124 C51E7400	3359	DB	24H,C51E7400H		
F128 58	3360	DB	28H,58H		
F129 891000	3361	DB	29H,891000H		
F12C 80FC02	3362	DB	2CH,0FC02H		
F12F 7210	3363	DB	2FH,7210H		
F131 0309	3364	DB	31H,0309H		
F133 80FC04	3365	DB	33H,80FC04H		
F136 7209	3366	DB	36H,7209H		
F138 0309	3367	DB	38H,0309H		
F13A 80FC07	3368	DB	3AH,80FC07H		
F13D 7202	3369	DB	3DH,7202H		
F13F 0309	3370	DB	3FH,0309H		
	3371	DB	0,0,0,0		
	3372	DB	0,0,0,0		
	3373	DB	0,0,0,0		
	3374	DB	0,0,0,0		
	3375	DB	0,0,0,0		
F141	3376	DB	0,0,0,0		
F141 50	3377	DB	41H,50H		
F142 32E4	3378	DB	42H,32E4H		
	3379	DB	0,0,0,0		
	3380	DB	0,0,0,0		
	3381	DB	0,0,0,0		
F144	3382	DB	0,0,0,0		
F144 8AC4	3383	DB	44H,8AC4H		

LOC	OBJ	LINE	SOURCE	LOC	OBJ	LINE	SOURCE
		3458	VIDEO_RETURN:			3533	CALL M16 ; OUTPUT THE VALUE TO THE 6845
F1C7		3459	POP DI	F21A EBCIFF		3534	RET ENDP
F1C7 5F		3460	POP SI	F219 C3		3535	-----
F1C8 5E		3461	POP DX			3536	; READ_CURSOR
F1C9 5D		3462	M15: ; VIDEO_RETURN_C			3537	; THIS ROUTINE READS THE CURRENT CURSOR VALUE FROM THE
F1CA		3463	POP CX			3538	6845, FORMATS IT, AND SENDS IT BACK TO THE CALLER
F1CA 59		3464	POP DX			3539	; INPUT
F1CB 5A		3465	POP DS			3540	; BH = PAGE OF CURSOR
F1CC 5F		3466	POP ES			3541	; OUTPUT
F1CD 07		3467	IRET			3542	; DX = ROW, COLUMN OF THE CURRENT CURSOR POSITION
F1CE CF		3468	SET_MODE ENDP			3543	; CX = CURRENT CURSOR MODE
		3469	-----			3544	-----
		3470	; SET_CTYPE	F21A		3545	READ_CURSOR PROC NEAR
		3471	; THIS ROUTINE SETS THE CURSOR VALUE	F21A 6A0F		3546	MOV BL,BH
		3472	; INPUT	F21C 32FF		3547	XOR BH,BH
		3473	; (CX) HAS CURSOR VALUE ON-START LINE, CL-STOP LINE	F21E D1E3		3548	SAL BX,1 ; WORD OFFSET
		3474	; OUTPUT	F220 68975000		3549	MOV DX,(BX+OFFSET_CURSOR_POSH)
		3475	; NONE	F224 6806A000	R	3550	MOV CX,CURSOR_MODE
		3476	-----	F228 5F		3551	POP DI
		3477	SET_CTYPE PROC NEAR	F229 5E		3552	POP SI
F1CF		3478	MOV AH,10 ; 6845 REGISTER FOR CURSOR SET	F22A 5B		3553	POP BX
F1CF 6A0A	R	3479	MOV CURSOR_MODE,CX ; SAVE IN DATA AREA	F22B 58		3554	POP AX ; DISCARD SAVE CX AND DX
F1D1 696E6000		3480	CALL M16 ; OUTPUT CX REG	F22C 58		3555	POP AX
F1D5 E06200		3481	JMP VIDEO_RETURN	F22D 1F		3556	POP DS
F1DB EBD0		3482	-----	F22E 07		3557	POP ES
		3483	;----- THIS ROUTINE OUTPUTS THE CX REGISTER TO THE 6845 REGS NAMED IN AH	F22F CF		3558	IRET
		3484	-----			3559	READ_CURSOR ENDP
F1DA		3485	M16: ; ADDRESS REGISTER			3560	; ACT_DISP_PAGE
F1DA 8B166300	R	3486	MOV CX,ADDR_6845 ; GET VALUE			3561	; THIS ROUTINE SETS THE ACTIVE DISPLAY PAGE, ALLOWING
F1DE BAC4		3487	OUT DX,AL ; REGISTER SET			3562	THE FULL USE OF THE RAM SET ASIDE FOR THE VIDEO ATTACHMENT
F1DE EE		3488	INC DX ; DATA REGISTER			3563	; INPUT
F1E1 42		3489	MOV AL,CH ; DATA			3564	; OUTPUT
F1E2 BAC5		3490	OUT DX,AL			3565	; AL HAS THE NEW ACTIVE DISPLAY PAGE
F1E4 EE		3491	DEC DX			3566	; THE 6845 IS RESET TO DISPLAY THAT PAGE
F1E5 4A		3492	DEC DX			3567	-----
F1E6 BAC4		3493	MOV AL,AH ; POINT TO OTHER DATA REGISTER	F230		3568	ACT_DISP_PAGE PROC NEAR
F1E8 F6C0		3494	INC AL ; SET FOR SECOND REGISTER	F230 426200	R	3569	MOV CX,ACTIVE_PAGE,AL ; SAVE ACTIVE PAGE VALUE
F1E8 EE		3495	OUT DX,AL	F233 8B06C000		3570	MOV CX,CRT_LEN ; GET SAVED LENGTH OF REGEN BUFFER
F1EB 42		3496	INC DX	F237 9B		3571	MOV CX,CRT_LEN ; CONVERT AL TO WORD
F1EE BAC1		3497	MOV AL,CL ; SECOND DATA VALUE	F238 50		3572	MOV AX
F1EE EE		3498	OUT DX,AL	F239 F7E1		3573	MOV AX
F1EF C3		3499	RET ; ALL DONE			3574	; SAVE PAGE VALUE
		3500	SET_CTYPE ENDP	F23C 334E00	R	3575	MUL CX,CRT_START,AX ; DISPLAY PAGE TIMES REGEN LENGTH
		3501	-----	F23E 8B0C0		3576	MOV CX,AX ; SAVE START ADDRESS FOR LATER REQUIREMENTS
		3502	; SET_CPOS	F240 D1F9		3577	SAR CX,1 ; DIVIDE BY 2 FOR 6845 HANDLING
		3503	; NEW X-1 VALUES PASSED	F242 B40C		3578	MOV AH,12 ; 6845 REGISTER FOR START ADDRESS
		3504	; THIS ROUTINE SETS THE CURRENT CURSOR POSITION TO THE	F244 E83FF		3579	CALL M16
		3505	; INPUT	F247 5B		3580	POP BX ; RECOVER PAGE VALUE
		3506	; DX = ROW,COLUMN OF NEW CURSOR	F248 D1E3		3581	SAL BX,1 ; *2 FOR WORD OFFSET
		3507	; BH = DISPLAY PAGE OF CURSOR	F24A 68B75000	R	3582	MOV AX,(BX+OFFSET_CURSOR_POSH) ; GET CURSOR FOR THIS PAGE
		3508	; CURSOR IS SET AT 6845 IF DISPLAY PAGE IS CURRENT DISPLAY	F24E E8B8FF		3583	CALL M18 ; SET THE CURSOR POSITION
		3509	; OUTPUT	F251 E973FF		3584	JMP VIDEO_RETURN
		3510	SET_CPOS PROC NEAR			3585	ACT_DISP_PAGE ENDP
		3511	MOV CL,BH			3586	; SET COLOR
		3512	XOR CH,CH			3587	-----
		3513	SAR CX,1			3588	; THIS ROUTINE WILL ESTABLISH THE BACKGROUND COLOR, THE OVERSCAN COLOR,
		3514	; USE INDEX REGISTER			3589	AND THE FOREGROUND COLOR SET FOR MEDIUM RESOLUTION GRAPHICS
		3515	MOV SI,CX			3590	; INPUT
		3516	MOV AX,(SI+OFFSET_CURSOR_POSH),DX ; SAVE THE POINTER			3591	; (BH) HAS COLOR ID
		3517	CHP ACTIVE_PAGE,BH			3592	IF BH=0, THE BACKGROUND COLOR VALUE IS SET
		3518	JNZ M17 ; SET_CPOS_RETURN			3593	FROM THE LOW BITS OF BL (0-31)
		3519	MOV AX,DX ; GET ROW/COLUMN TO AX			3594	IF BH=1, THE PALLETTE SELECTION IS MADE
		3520	CALL M18 ; CURSOR_SET			3595	BASED ON THE LOW BIT OF BL:
		3521	CALL M18 ; SET_CPOS_RETURN			3596	0 = GREEN, RED, YELLOW FOR COLORS 1,2,3
		3522	JMP VIDEO_RETURN			3597	1 = BLUE, CYAN, MAGENTA FOR COLORS 1,2,3
		3523	SET_CPOS ENDP			3598	; (BL) HAS THE COLOR VALUE TO BE USED
		3524	-----			3599	-----
		3525	;----- SET CURSOR POSITION, AX HAS ROW/COLUMN FOR CURSOR			3600	; THE COLOR SELECTION IS UPDATED
		3526	-----			3601	-----
		3527	M18 PROC NEAR			3602	SET_COLOR PROC NEAR
		3528	CALL POSITION			3603	MOV DX,ADDR_6845 ; I/O PORT FOR PALLETTE
		3529	MOV CX,AX			3604	ADD DX,5 ; OVERSCAN PORT
		3530	ADD AX,CRT_START			3605	MOV AL,CRT_PALLETTE ; GET THE CURRENT PALLETTE VALUE
		3531	SAR CX,1			3606	OR BH,BH ; IS THIS COLOR 0?
		3532	MOV AH,16			3607	
		3533	MOV AX,16				
		3534	MOV AX,16				
		3535	MOV AX,16				
		3536	MOV AX,16				
		3537	MOV AX,16				
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		3688	MOV AX,16				</

LOC OBJ	LINE	SOURCE	LOC OBJ	LINE	SOURCE
F260 750E	3608	JNZ M20 ; OUTPUT COLOR 1	F2A1 750B	3604	JC NI ; HANDLE SEPARATELY
	3609	;	F2A3 80FC07	3605	CHP AH:7 ; TEST FOR BH CARD
	3610	;	F2A6 7403	3606	JE NI ; GRAPHICS UP
F262 24E0	3611	;	F2A8 E9F301	3607	JMP NI: ; UP_CONTINUE
F264 0E31F	3612	AND AL,0FH ; TURN OFF LOW 5 BITS OF CURRENT	F2AB 53	3608	PUSH BX ; SAVE LEFT ATTRIBUTE IN BH
F267 0AC3	3613	AND BL,0FH ; TURN OFF HIGH 3 BITS OF INPUT VALUE	F2AC 06C1	3609	MOV AX:CX ; UPPER LEFT POSITION
F269	3614	OR AL,BL ; INPUT VALUE INTO REGISTER	F2AE E81900	3610	CALL SCROLL_POSITION ; DO SETUP FOR SCROLL
F269 EE	3615	MI9: OUT DX:AL ; output color selection to 349 port	F2B1 7433	3611	JZ N7 ; BLANK FIELD
F26A 426A00	3616	OUT CRT_PALETTE:AL ; SAVE THE COLOR VALUE	F2B3 03F0	3612	ADD SI,AX ; FROM ADDRESS
F26B E97FF	3617	JMP VIDEO_RETURN	F2B5 04E6	3613	MOV AH:0H ; 8 ROWS IN BLOCK
	3618	;	F2B7 24E3	3614	SUB AH,BL ; 8 ROWS TO BE MOVED
	3619	;	F2B9 E97500	3615	CALL N10 ; MOVE ONE ROW
F270	3620	;	F2BC 03F5	3616	ADD SI,BP
F270 240F	3621	AND AL,00FH ; TURN OFF PALETTE SELECT BIT	F2BD 03F0	3617	ADD DI,BP
F272 20E8	3622	SHR BL,1 ; TEST THE LOW ORDER BIT OF BL	F2C0 FECC	3618	DEC AH ; COUNT OF LINES TO MOVE
F274 73F3	3623	JNC M19 ; ALREADY DONE	F2C2 75F5	3619	JZ N2 ; ROW_LOOP
F276 0C00	3624	OR AL,20H ; TURN ON PALETTE SELECT BIT	F2C4 58	3620	POP AX ; RECOVER ATTRIBUTE IN AH
F276 E8E7	3625	JMP M19 ; GO DO IT	F2C5 8620	3621	MOV AL,' ' ; FILL WITH BLANKS
	3626	;	F2C7	3622	;
	3627	SET_COLOR ENDP	F2C7 E87000	3623	CALL H11 ; CLEAR THE ROW
	3628	;	F2CA 03F0	3624	ADD DI,BP ; POINT TO NEXT LINE
	3629	;	F2CC FECC	3625	DEC BL ; COARTER OF LINES TO SCROLL
	3630	;	F2CE 75F7	3626	JNZ N4 ; CLEAR_LOOP
	3631	;	F2D0	3627	;
F27A	3632	VIDEO_STATE PROC NEAR	F2D0 8A6400	3628	MOV AX:DATA ; GET LOCATION
F27A 0A26A00	3633	MOV AN:BIT PTR CRT_COLS ; GET NUMBER OF COLUMNS	F2D1 3711	3629	MOV DS:AX ; GET MODE.7
F27E 0A4900	3634	MOV AL:CRT_MODE ; GET CURRENT MODE	F2D3 8E0A	3630	CHP CRT_MODE:7 ; IS THIS THE BLACK AND WHITE CARD
F281 8A36200	3635	MOV BL:ACTIVE_PAGE ; GET CURRENT ACTIVE PAGE	F2D4 7407	3631	JE N6 ; IF SO, SKIP THE MODE RESET
F286 5F	3636	POP DI ; RECOVER REGISTERS	F2D6 A8500	3632	MOV AL:CRT_MODE:SET ; GET THE VALUE OF THE MODE SET
F286 SE	3637	POP SI ; DISCARD SAVED BX	F2D8 0A0803	3633	MOV DX:0308H ; ALWAYS SET COLOR CARD PORT
F286 5E	3638	POP CX ; RETURN TO CALLER	F2DE EE	3634	OUT DX:AL
F287 59	3639	JMP M15	F2E3	3635	;
F28B E97FF	3640	VIDEO_STATE ENDP	F2E3 87E1FE	3636	;
	3641	;	F2E6	3637	;
	3642	;	F2E6 80DE	3638	MOV BL,0H ; BLANK_FIELD
	3643	;	F2E8 E80A	3639	MOV H3 ; GO CLEAR THAT AREA
	3644	;		3640	SCROLL_UP ENDP
	3645	;		3641	;
	3646	;		3642	;
	3647	;		3643	;
	3648	;		3644	;
	3649	;		3645	;
	3650	;		3646	;
	3651	;		3647	;
	3652	;		3648	;
	3653	;		3649	;
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	3801	;		3797	;
	3802	;		3798	;
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	3804	;		3800	;
	3805	;		3801	;
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	3807	;		3803	;
	3808	;		3804	;
	3809	;		3805	;
	3810	;		3806	;
	3811	;		3807	;
	3812	;		3808	;
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	3877	;			

LOC OBJ	LINE	SOURCE
F328 06	3760	PUSH ES
F32C 1F	3761	POP D5
F32D 80F00	3762	CHP BL,0
F330 C3	3763	RET
	3764	SCROLL_POSITION ENDP
	3765	-----
F331	3766	MOV_BM, NEAR
F331 8ACA	3767	MOV CL,DL
F333 36	3768	PUSH SI
F334 57	3769	PUSH DI
F335 F3	3770	REP MOVSW
F336 A5	3771	REP MOVSW
F337 5F	3772	POP DI
F338 5E	3773	POP SI
F339 C3	3774	RET
	3775	ENDP
	3776	N10
	3777	-----
F33A	3778	MOV CL,DL
F33A 8ACA	3779	PUSH DI
F33C 57	3780	REP MOVSW
F33D F3	3781	REP MOVSW
F33E AB	3782	POP DI
F33F 5F	3783	RET
F340 C3	3784	ENDP
	3785	N11
	3786	-----
F341	3787	MOV CL,DL
F341 FD	3788	PUSH DI
F342 8A0B	3789	REP MOVSW
F344 80F00	3790	RET
F347 720B	3791	CHP AN,7
F349 80F00	3792	RET
F34C 7403	3793	CHP AN,7
F34E E9A01	3794	CHP AN,7
F351	3795	MOV AX,DX
F351 53	3796	CALL SCROLL_POSITION
F352 8BC2	3797	CALL SCROLL_POSITION
F354 E03FF	3798	CALL SCROLL_POSITION
F357 7420	3799	CALL SCROLL_POSITION
F359 28F0	3800	CALL SCROLL_POSITION
F35B 8A0E	3801	CALL SCROLL_POSITION
F35D 2A03	3802	CALL SCROLL_POSITION
F35F	3803	CALL SCROLL_POSITION
F35F E0CFF	3804	CALL SCROLL_POSITION
F362 28F5	3805	CALL SCROLL_POSITION
F364 28F0	3806	CALL SCROLL_POSITION
F366 FECC	3807	CALL SCROLL_POSITION
F368 75F5	3808	CALL SCROLL_POSITION
F36A	3809	CALL SCROLL_POSITION
F36A 5B	3810	CALL SCROLL_POSITION
F36B 8020	3811	CALL SCROLL_POSITION
F36D	3812	CALL SCROLL_POSITION
F36D E0CAFF	3813	CALL SCROLL_POSITION
F370 28F0	3814	CALL SCROLL_POSITION
F372 FE0B	3815	CALL SCROLL_POSITION
F374 75F7	3816	CALL SCROLL_POSITION
F376 E057FF	3817	CALL SCROLL_POSITION
F379	3818	CALL SCROLL_POSITION
F379 8A0E	3819	CALL SCROLL_POSITION
	3820	CALL SCROLL_POSITION
	3821	CALL SCROLL_POSITION
	3822	CALL SCROLL_POSITION
	3823	CALL SCROLL_POSITION
	3824	CALL SCROLL_POSITION
	3825	CALL SCROLL_POSITION
	3826	CALL SCROLL_POSITION
	3827	CALL SCROLL_POSITION
	3828	CALL SCROLL_POSITION
	3829	CALL SCROLL_POSITION
	3830	CALL SCROLL_POSITION
	3831	CALL SCROLL_POSITION
	3832	CALL SCROLL_POSITION
	3833	CALL SCROLL_POSITION

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LOC OBJ	LINE	SOURCE	LOC OBJ	LINE	SOURCE
F400 00E2FE	4062	AND DL,0FEH ; STRIP OFF ODD/EVEN BIT	F4A7 2801	4137	SUB DX,CK
F403 F6E2	4063	MUL DL ; AX HAS ADDRESS OF 1ST BYTE OF INDICATED ROW	F4A9 81C20101	4138	ADD DX,101H
F405 5A	4064	POP DX ; RECOVER IT	F4AD 00E6	4139	SAL DH,1
F406 F6C201	4065	TEST DL,1 ; TEST FOR EVEN/ODD	F4AF 00E6	4140	SAL DH,1
F409 7403	4066	JZ R4 ; JUMP IF EVEN ROW		4141	J----- DETERMINE CRT MODE
F40B 050020	4067	ADD AX,2000H ; OFFSET TO LOCATION OF ODD ROWS		4142	J-----
F40E	4068	EVEN_ROW		4143	CHP CRT_MODE,6
F40F 0070	4069	MOV SI,AX ; MOVE POINTER TO SI		4144	JNC R7
F470 5A	4070	POP AX ; RECOVER AL VALUE		4145	J-----
F471 8001	4071	MOV DX,CK ; COLUMN VALUE TO DX		4146	J-----
	4072	J----- DETERMINE GRAPHICS MODE CURRENTLY IN EFFECT		4147	J-----
	4073	J-----		4148	SAL DL,1
	4074	J-----		4149	SAL DL,1
	4075	J-----		4150	J-----
	4076	J-----		4151	J-----
	4077	J-----		4152	J-----
	4078	J-----		4153	J-----
	4079	J-----		4154	J-----
	4080	J-----		4155	J-----
	4081	J-----		4156	J-----
	4082	J-----		4157	J-----
	4083	J-----		4158	J-----
	4084	J-----		4159	J-----
	4085	J-----		4160	J-----
	4086	J-----		4161	J-----
	4087	J-----		4162	J-----
	4088	J-----		4163	J-----
	4089	J-----		4164	J-----
	4090	J-----		4165	J-----
	4091	J-----		4166	J-----
	4092	J-----		4167	J-----
	4093	J-----		4168	J-----
	4094	J-----		4169	J-----
	4095	J-----		4170	J-----
	4096	J-----		4171	J-----
	4097	J-----		4172	J-----
	4098	J-----		4173	J-----
	4099	J-----		4174	J-----
	4100	J-----		4175	J-----
	4101	J-----		4176	J-----
	4102	J-----		4177	J-----
	4103	J-----		4178	J-----
	4104	J-----		4179	J-----
	4105	J-----		4180	J-----
	4106	J-----		4181	J-----
	4107	J-----		4182	J-----
	4108	J-----		4183	J-----
	4109	J-----		4184	J-----
	4110	J-----		4185	J-----
	4111	J-----		4186	J-----
	4112	J-----		4187	J-----
	4113	J-----		4188	J-----
	4114	J-----		4189	J-----
	4115	J-----		4190	J-----
	4116	J-----		4191	J-----
	4117	J-----		4192	J-----
	4118	J-----		4193	J-----
	4119	J-----		4194	J-----
	4120	J-----		4195	J-----
	4121	J-----		4196	J-----
	4122	J-----		4197	J-----
	4123	J-----		4198	J-----
	4124	J-----		4199	J-----
	4125	J-----		4200	J-----
	4126	J-----		4201	J-----
	4127	J-----		4202	J-----
	4128	J-----		4203	J-----
	4129	J-----		4204	J-----
	4130	J-----		4205	J-----
	4131	J-----		4206	J-----
	4132	J-----		4207	J-----
	4133	J-----		4208	J-----
	4134	J-----		4209	J-----
	4135	J-----		4210	J-----
	4136	J-----		4211	J-----
				4212	J-----

LOC OBJ	LINE	SOURCE	LOC OBJ	LINE	SOURCE
74FF 0878	4213	MOV DI,AX	F56B F3	4287	REP MOVSB ; MOVE THE ODD FIELD
	4214	;	F56C A4	4288	POP DI ; POINTERS BACK
	4215	;	F56D 5F	4289	POP SI ; RETURN TO CALLER
F501 2B01	4216	SUB DX,CX	F56E 3E	4290	RET
F503 81C20101	4217	ADD DX,101H	F56F C3	4291	ENDP
F507 0066	4218	SAL DH,1			
F509 0066	4219	SAL DH,1			
	4220	;			
	4221	;			
	4222	;			
	4223	;			
F500 803E49006	4224	CMP CRT_MODE,6	F570	4292	;
F510 7305	4225	JNC R12	F570 0ACA	4293	;
	4226	;	F572 57	4294	;
	4227	;	F573 F3	4295	;
F512 00E2	4228	SAL DL,1	F574 AA	4296	;
F516 01E7	4229	SAL DL,1	F575 5F	4297	;
F516 47	4230	INC DI	F576 81C70020	4298	;
	4231	;	F57A 57	4299	;
	4232	;	F57B 0ACA	4300	;
	4233	;	F57D F3	4301	;
	4234	;	F57E AA	4302	;
F517 06	4235	PUSH ES	F57F 5F	4303	;
F518 1F	4236	POP DS	F580 C3	4304	;
F519 24E0	4237	SUB CH,CH		4305	;
F51B 81C7F000	4238	ADD DI,240		4306	;
F51F 00E3	4239	SAL BL,1		4307	;
F521 00E3	4240	JZ R16		4308	;
F523 742E	4241	MOV AL,BL		4309	;
F525 8AC3	4242	MOV AH,80		4310	;
F527 8A90	4243	MUL AH		4311	;
F529 F4E4	4244	MOV SI,DI		4312	;
F52B 0877	4245	SUB SI,AX		4313	;
F52D 2B10	4246	MOV AH,DI		4314	;
F52F 0A66	4247	SUB AH,BL		4315	;
F531 2A13	4248	;		4316	;
	4249	;		4317	;
F533	4250	;		4318	;
F533 E82100	4251	CALL R17		4319	;
F536 81EE5020	4252	SUB SI,2000H+80		4320	;
F53A 81EF5020	4253	SUB SI,2000H+80		4321	;
F53E FECC	4254	DEC AH		4322	;
F540 75F1	4255	JNZ R13		4323	;
	4256	;		4324	;
	4257	;		4325	;
F542	4258	;		4326	;
F542 8AC7	4259	MOV AL,BH		4327	;
F544	4260	;		4328	;
F544 E82700	4261	CALL R18		4329	;
F547 81EF5020	4262	SUB DI,2000H+80		4330	;
F54B FECD	4263	DEC BL		4331	;
F54D 75F5	4264	JZ R15		4332	;
F54F FC	4265	CJZ		4333	;
F550 E794FC	4266	JMP VIDEO_RETURN		4334	;
	4267	;		4335	;
F553	4268	;		4336	;
F553 8ADE	4269	MOV BL,DI		4337	;
F555 E8E8	4270	JMP R14	F581	4338	;
	4271	;	F581 0A00	4339	;
	4272	;	F583 50	4340	;
	4273	;		4341	;
	4274	;		4342	;
	4275	;		4343	;
F557	4276	PROC NEAR	F584 E08501	4344	;
F557 0ACA	4277	MOV CL,DL	F587 8078	4345	;
F559 54	4278	PUSH SI		4346	;
F55A 57	4279	PUSH DI		4347	;
F55B F3	4280	REP MOVSB		4348	;
F55C A4	4281	POP DI	F589 58	4349	;
F55E 5C	4282	POP SI	F58A 3C80	4350	;
F55F 81C40020	4283	ADD AX,31200H	F58C 7306	4351	;
F563 81C70020	4284	ADD AX,31200H		4352	;
F567 56	4285	PUSH SI		4353	;
F568 57	4286	PUSH DI		4354	;
F569 0ACA	4287	MOV CL,DL		4355	;
	4288	;		4356	;
	4289	;		4357	;
	4290	;		4358	;

LOC OBJ	LINE	SOURCE	LOC OBJ	LINE	SOURCE
F594	4359	;----- IMAGE IS IN SECOND HALF, IN USER RAM	F607 3C31	4435	AND AX,BX ; CONVERT TO COLOR
F594 2C80	4361	S1:	F609 4C280	4436	TEST DL,00H ; AGAIN, IS THIS XOR FUNCTION
F594 IE	4362	SUB AL,00H ; EXTEND CHAR	JZ SL	4437	; NO, JUST STORE THE VALUES
F597 20F6	4363	PUSH DS	XOR AH,ESI+2000H	4438	; AND WITH SECOND HALF
F599 80E0	4364	SUB SI,S1	XOR AL,ESI+2000H	4439	; AND WITH SECOND HALF
F59B C5367C00	4365	MOV DS,SI	S11:		
F59F 80CA	4366	MOV DS,SI	MOV ES:DI+2000H+1,AL	4440	; STORE IN SECOND PORTION OF BUFFER
F5A1 IF	4367	LOS SI,EXT_PTR	ADD DI,60	4441	; POINT TO NEXT LOCATION
F5A2 52	4368	MOV DX,DS	DEC DH	4442	; KEEP GOING
	4369	ASSUME DS:DATA	JNZ S9	4443	; RECOVER CODE POINTER
	4370	POP DS	POP SI	4444	; RECOVER REGEN POINTER
	4371	PUSH DX	ADD DI,2	4445	; POINT TO NEXT CHAR POSITION
	4372	;----- DETERMINE GRAPHICS MODE IN OPERATION	LOOP S8	4446	; MORE TO WRITE
	4373	S2:	JMP VIDEO_RETURN	4447	
	4374	S3:	GRAPHICS_WRITE ENOP	4448	
F5A3 D1E0	4375	SAL AX,1	; GRAPHICS READ	4449	
F5A5 D1E0	4376	SAL AX,1	; GRAPHICS READ	4450	
F5A7 D1E0	4377	SAL AX,1	; GRAPHICS READ	4451	
F5A9 03F0	4378	ADD SI,AX	GRAPHICS_READ PROC NEAR	4452	
F5AB 803C-00006	4379	CHP CRT_MODE.6	; CONVERTED TO OFFSET IN REGEN	4453	
F5B0 IF	4380	POP DS	MOV SI,AX	4454	; SAVE IN SI
F5B1 72C	4381	POP DS	SUB SP,8	4455	; ALLOCATE SPACE TO SAVE THE READ CODE POINT
	4382	JC S7	MOV BP,SP	4456	; POINTER TO SAVE AREA
	4383	;----- HIGH RESOLUTION MODE		4457	
F5B3	4384	S3:	;----- DETERMINE GRAPHICS MODES	4458	
F5B3 57	4385	PUSH DI	CHP CRT_MODE.6	4459	
F5B4 56	4386	PUSH SI	PUSH ES	4460	
F5B5 8A04	4387	MOV DH,4	PUSH DS	4461	
F5B7	4388	MOV DH,4	JC S13	4462	
F5B7 AC	4389	LOOP S8		4463	
F5B8 FAC300	4390	TEST BL,80H		4464	
F5B8 7516	4391	JNZ S6		4465	
F5B8 AA	4392	STOSB		4466	
F5B8 AC	4393	LOOP S8		4467	
F5B8	4394	MOV ES:DI+2000H-1,AL		4468	
F5B8 26A065FF1F	4395	ADD DI,79		4469	
F5C4 7C7AF	4396	DEC DH		4470	
F5C7 FECE	4397	JNZ S4		4471	
F5C9 75EC	4398	POP SI		4472	
F5CB 5E	4399	POP SI		4473	
F5CC 5F	4400	POP DI		4474	
F5CD 47	4401	INC DI		4475	
F5CE E2E3	4402	LOOP S3		4476	
F5D0 E9F4F8	4403	JMP VIDEO_RETURN		4477	
F603	4404	XOR AL,ESI+1011		4478	
F603 263205	4405	STOSB		4479	
F606 AA	4406	MOV DS,SI		4480	
F607 AC	4407	MOV DS,SI		4481	
F608 263205FF1F	4408	XOR AL,ESI+2000H-1,AL		4482	
F608 E8E0	4409	JMP S5		4483	
F60F	4410	;----- MEDIUM RESOLUTION WRITE		4484	
F60F 8A03	4411	MOV DL,BL		4485	
F611 D1E7	4412	SAL DI,1		4486	
F613 E80100	4413	CALL S19		4487	
F616	4414	PUSH DI		4488	
F616 57	4415	MOV SI		4489	
F617 56	4416	MOV SI		4490	
F618 8A04	4417	MOV SI		4491	
F61A	4418	MOV SI		4492	
F61A 57	4419	MOV SI		4493	
F61B 56	4420	MOV SI		4494	
F61C 8A04	4421	MOV SI		4495	
F61E AC	4422	MOV SI		4496	
F61E E8E0C0	4423	CALL S21		4497	
F61E 23E3	4424	AND AX,BX		4498	
F61F 8A04	4425	MOV SI		4499	
F620 8A04	4426	MOV SI		4500	
F621 7A07	4427	JC S10		4501	
F622 263225	4428	XOR AH,ESI+1011		4502	
F623 26324501	4429	XOR AL,ESI+1011		4503	
F62C 268055	4430	MOV ES:DI+1,AL		4504	
F62C 268055	4431	MOV ES:DI+1,AL		4505	
F62C 268055	4432	MOV ES:DI+1,AL		4506	
F62C AC	4433	CALL S21		4507	
F62C E8C500	4434	CALL S21		4508	
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LOC OBJ	LINE	SOURCE	LOC OBJ	LINE	SOURCE
F689 57	4511	PUSH DT	F689 57	4586	SHL CX,1
F68A 800000	4512	MOV CX,0	F689 58	4587	JNC S22
F68D F3	4513	REPZ CMPSB	F689 59	4588	MOV AX,DX
F68E A6			F689 5A	4589	POP BX
F68F 5F			F689 5B	4590	POP CX
F690 5E	4514	POP DI	F689 5C	4591	POP DX
F691 741E	4515	POP SI	F689 5D	4592	RET
F693 F4E0	4516	JZ S10	F689 5E	4593	ENDP
F695 83C700	4517	INC AL		4594	-----
F696 7404	4518	ADC DI,0		4595	! REG_READ_BYTE
F697 750D	4519	DEC DX		4596	! THIS ROUTINE WILL TAKE 2 BYTES FROM THE REGEN BUFFER.
	4520	JNC S17		4597	! COMPARE AGAINST THE CURRENT FOREGROUND COLOR, AND PLACE
	4521			4598	! THE CORRESPONDING ON/OFF BIT PATTERN INTO THE CURRENT
	4522			4599	! POSITION IN THE SAVE AREA
	4523			4600	! ENTRY --
	4524			4601	! SI:05 = POINTER TO REGEN AREA OF INTEREST
	4525			4602	! BX = EXPANDED FOREGROUND COLOR
	4526			4603	! BP = POINTER TO SAVE AREA
	4527			4604	! EXIT --
	4528			4605	! BP IS INCREMENT AFTER SAVE
	4529			4606	!-----
	4530			4607	PROC NEAR
	4531			4608	MOV AX,[SI]
	4532			4609	MOV AX,[SI+1]
	4533			4610	MOV CX,0000H
	4534			4611	MOV DL,0
	4535			4612	SEN:
	4536			4613	TEST AX,CX
	4537			4614	CLC
	4538			4615	JZ S25
	4539			4616	STC
	4540			4617	RCL DL,1
	4541			4618	SHR CX,1
	4542			4619	SHR CX,1
	4543			4620	JNC S24
	4544			4621	MOV [BP+1],0
	4545			4622	INC BP
	4546			4623	RET
	4547			4624	ENDP
	4548			4625	! V4 POSITION
	4549			4626	! THIS ROUTINE TAKES THE CURSOR POSITION CONTAINED IN
	4550			4627	! THE MEMORY LOCATION, AND CONVERTS IT INTO AN OFFSET
	4551			4628	! INTO THE REGEN BUFFER, ASSUMING ONE BYTE/CHAR.
	4552			4629	! FOR REGEN RESOLUTION GRAPHICS, THE NUMBER MUST
	4553			4630	! BE DOUBLED.
	4554			4631	! SAVE REGISTER
	4555			4632	! ENTRY -- NO REGISTERS, MEMORY LOCATION CURSOR_POSN IS USED
	4556			4633	! EXIT--
	4557			4634	! AX CONTAINS OFFSET INTO REGEN BUFFER
	4558			4635	!-----
	4559			4636	PROC NEAR
	4560			4637	MOV AX,CURSOR_POSN
	4561			4638	GRAPH_POSN LABEL NEAR
	4562			4639	PUSH BX
	4563			4640	MOV DX,AX
	4564			4641	MOV AL,AX
	4565			4642	MUL BYTE PTR CRT_COLS
	4566			4643	SHL AX,1
	4567			4644	SHL AX,1
	4568			4645	SUB DX,BX
	4569			4646	ADD AX,DX
	4570			4647	POP BX
	4571			4648	RET
	4572			4649	ENDP
	4573			4650	!-----
	4574			4651	! WRITE_TTY
	4575			4652	! THIS INTERFACE PROVIDES A TELETYPE LIKE INTERFACE TO THE
	4576			4653	! VIDEO CARD. THE INPUT CHARACTER IS WRITTEN TO THE CURRENT
	4577			4654	! CURSOR POSITION, AND THE CURSOR IS MOVED TO THE NEXT POSITION.
	4578			4655	! IF THE CURSOR LEAVES THE LAST COLUMN OF THE FIELD, THE COLUMN
	4579			4656	! IS SET TO ZERO, AND THE ROW VALUE IS INCREMENTED. IF THE ROW
	4580			4657	! ROW VALUE LEAVES THE FIELD, THE CURSOR IS PLACED ON THE LAST ROW,
	4581			4658	! FIRST COLUMN, AND THE ENTIRE SCREEN IS SCROLLED UP ONE LINE.
	4582			4659	! WHEN THE SCREEN IS SCROLLED UP, THE ATTRIBUTE FOR FILLING THE
	4583			4660	! NEXT BLANKED LINE IS READ FROM THE CURSOR POSITION ON THE PREVIOUS
	4584			4661	! LINE BEFORE THE SCROLL, IN CHARACTER MODE. IN GRAPHICS MODE,

LOC OBJ	LINE	SOURCE	LOC OBJ	LINE	SOURCE
	4662	1 THE 0 COLOR IS USED.		4738	JMP VIDEO_RETURN ; RETURN TO CALLER
	4663	1 ENTRY --		4739	UM: ; SET-CURSOR-INC
	4664	1 (AM) = CURRENT CRT MODE		4740	INC DH ; SET-CURSOR
	4665	1 NOTE THAT BACK SPACE, CAR RET, BELL AND LINE FEED ARE HANDLED		4741	MOV AH,2 ; SET-CURSOR
	4666	1 AS COMMANDS RATHER THAN AS DISPLAYABLE GRAPHICS		4742	JMP UA ; ESTABLISH THE NEW CURSOR
	4667	1 (BL) = FOREGROUND COLOR FOR CHAR WRITE IF CURRENTLY IN A GRAPHICS MODE		4743	
	4668	1 EXIT --		4744	
	4669	1 ALL REGISTERS SAVED		4745	
	4670	1		4746	
	4671	1 ASSUME CS:CODE,DS:DATA		4747	
	4672	WRITE_TTY PROC NEAR		4748	
	4673	PUSH AX ; SAVE REGISTERS		4749	
	4674	PUSH AX ; SAVE CHAP TO WRITE		4750	
	4675	MOV AH,3 ; READ THE CURRENT CURSOR POSITION		4751	
	4676	INT 10H ; RECOVER CHAP		4752	
	4677	POP AX ;		4753	
	4678			4754	
	4679			4755	
	4680	1----- DX NOW HAS THE CURRENT CURSOR POSITION		4756	
	4681			4757	
	4682	CHP AL,8 ; IS IT A BACKSPACE		4758	
	4683	JE U0 ; BACK SPACE		4759	
	4684	CHP AL,0DH ; IS IT CARRIAGE RETURN		4760	
	4685	JE U0 ; CAR RET		4761	
	4686	CHP AL,0AH ; IS IT A LINE FEED		4762	
	4687	JE U0 ; LINE FEED		4763	
	4688	CHP AL,07H ; IS IT A BELL		4764	
	4689	JE U1 ; BELL		4765	
	4690			4766	
	4691	1----- WRITE THE CHAR TO THE SCREEN		4767	
	4692			4768	
	4693	MOV BH,ACTIVE_PAGE ; GET THE CURRENT ACTIVE PAGE		4769	
	4694	MOV AH,10 ; WRITE CHAR ONLY		4770	
	4695	CALL 1 ; ONLY ONE CHAR		4771	
	4696	INT 10H ; WRITE THE CHAR		4772	
	4697			4773	
	4698	1----- POSITION THE CURSOR FOR NEXT CHAR		4774	
	4699			4775	
	4700	INC DL		4776	
	4701	CHP DL,01H ; TEST FOR COLUMN OVERFLOW		4777	
	4702	JNZ U7 ; SET CURSOR		4778	
	4703	MOV DL,0 ; COLUMN FOR CURSOR		4779	
	4704	CHP DH,24		4780	
	4705	JNZ U6 ; SET CURSOR-INC		4781	
	4706			4782	
	4707	1----- SCROLL REQUIRED		4783	
	4708			4784	
	4709			4785	
	4710	MOV AH,2		4786	
	4711	MOV BH,0		4787	
	4712	INT 10H ; SET THE CURSOR		4788	
	4713			4789	
	4714	1----- DETERMINE VALUE TO FILL WITH DURING SCROLL		4790	
	4715			4791	
	4716	MOV AL,CRT_MODE ; GET THE CURRENT MODE		4792	
	4717	CHP AL,4		4793	
	4718	JC U2 ; READ-CURSOR		4794	
	4719	CHP AL,7		4795	
	4720	MOV BH,0 ; FILL WITH BACKGROUND		4796	
	4721	JNE U3 ; SCROLL-UP		4797	
	4722			4798	
	4723	U2: ; READ-CURSOR		4799	
	4724	MOV AH,8		4800	
	4725	INT 10H ; READ CHAR/ATTR AT CURRENT CURSOR		4801	
	4726	MOV BH,AH ; STORE IN BH		4802	
	4727			4803	
	4728	U3: ; SCROLL-UP		4804	
	4729	MOV AH,01H ; SCROLL ONE LINE		4805	
	4730	CALL 0 ; UPPER LEFT CORNER		4806	
	4731	MOV DH,24 ; LOWER RIGHT ROW		4807	
	4732	MOV DL,01H ; LOWER RIGHT COLUMN		4808	
	4733	DEC DL		4809	
	4734	U1: ; VIDEO-CALL-RETURN		4810	
	4735	INT 10H ; SCROLL UP THE SCREEN		4811	
	4736	U5: ; TTY-RETURN		4812	
	4737	POP AX ; RESTORE THE CHARACTER		4813	
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LOC	OBJ	LINE	SOURCE	LOC	OBJ	LINE	SOURCE
4615	7C1 BAC4		MOV AL,AX			4891	POP DX
4616	7C3 EE		OUT DX,AL			4892	POP DI
4617	7C4 42		INC DX			4893	POP SI
4618	7C5 EC		IN AL,DX			4894	POP DS
4619	7C6 9AE8		MOV CH,AL			4895	POP DS
4620	7C8 4A		DEC CH			4896	POP DS
4621	7C9 FEF4		INC AH			4897	POP DS
4622	7CB BAC4		MOV AL,AX			4898	POP ES
4623	7CD EE		OUT DX,AL			4899	POP ES
4624	7CE 42		INC DX			4900	INBT
4625	7CF EC		IN AL,DX			4901	READ_LRN ENOP
4626	7D0 8A45		MOV AH,CH			4902	INT 12
4627			----- AX HAS THE VALUE READ IN FROM THE 6845			4903	MEMORY_SIZE_DTERMINE
4628						4904	
4629						4905	
4630						4906	
4631	F702 BALE4900	R	MOV BL,CRT_MODE			4907	
4632	F706 2AFF		SUB BH,BH			4908	
4633	F707 2EBAFA1F7	R	MOV BL,CS-VILBYJ			4909	
4634	F700 2EC3		SUB AX,BX			4910	
4635	F70F 2B064E00	R	SUB AX,CRT_START			4911	
4636	F7E3 7903		JNS V2			4912	
4637	F7E5 800000		MOV AX,0			4913	
4638			----- DETERMINE MODE OF OPERATION			4914	
4639						4915	
4640	F7E6		V2:			4916	
4641	F7E8 B103		MOV CL,3			4917	
4642	F7EA 6D3E490004	R	CHP CRT_MODE,4			4918	
4643	F7E7 7E2A		JB V4			4919	
4644	F7E1 8D3E490007	R	CHP CRT_MODE,7			4920	
4645	F7E6 7423		JE V4			4921	
4646			----- GRAPHICS MODE			4922	
4647						4923	
4648	F7E9 B226		MOV DL,40			4924	
4649	F7FA F6F2		DIV DL			4925	
4650			----- DETERMINE GRAPHIC ROM POSITION			4926	
4651						4927	
4652						4928	
4653	F7FC BAE8		MOV CH,AL			4929	
4654	F7FE 02D0		AOD CH,CH			4930	
4655	F800 BADC		MOV BL,AH			4931	
4656	F802 2AFF		SUB BH,BH			4932	
4657	F804 8D3E490006	R	CHP CRT_MODE,6			4933	
4658	F809 7504		JBE V3			4934	
4659	F80B B104		MOV CL,4			4935	
4660	F80D 00E4		SAL AH,1			4936	
4661	F80F		V3:			4937	
4662	F80F 03E3		SHL BX,CL			4938	
4663			----- DETERMINE ALPHA CHAR POSITION			4939	
4664						4940	
4665						4941	
4666	F811 BAC4		MOV DL,AH			4942	
4667	F813 6AF0		MOV DH,AL			4943	
4668	F815 00E		SHR DH,1			4944	
4669	F817 00FE		SHR DH,1			4945	
4670	F819 6B12		JMP SHORT V5			4946	
4671						4947	
4672			----- ALPHA MODE ON LIGHT PEN			4948	
4673						4949	
4674	F81B F6364A00	R	V4:			4950	
4675	F81F 6AF0		MOV DL,AH			4951	
4676	F821 BAC4		MOV DL,AH			4952	
4677	F823 D2E0		SAL AL,CL			4953	
4678	F825 BAE8		MOV CH,AL			4954	
4679	F827 BADC		MOV BL,AH			4955	
4680	F829 32FF		XOR BH,BH			4956	
4681	F82B D3E3		SAL BX,CL			4957	
4682	F82D 8401		MOV AH,1			4958	
4683	F82F		V5:			4959	
4684	F82F 8016A1300	R	PUSH DX			4960	
4685	F830 816A1300		AOD DX,7			4961	
4686	F831 816A1300		OUT DX,AL			4962	
4687	F832 EE					4963	
4688						4964	
4689						4965	
4690						4966	

LOC OBJ	LINE	SOURCE	LOC OBJ	LINE	SOURCE
F640	4967	EQUIPMENT	F685	5043	MOTOR_ON PROC HEAD
F640 F8	4968	STI		5044	;
F64E 1E	4969	PUSH DS		5045	;
F64F 8E4000	4970	MOV AX,DATA		5046	;
F652 8E0B	4971	MOV DS,AX		5047	;
F654 A11000	4972	MOV AX,EQUIP_FLAG		5048	IN AL,PORT_B
F657 1F	4973	POP DS		5049	AND AL,NOT 0BH
F658 CF	4974	IRET		5050	PORT_D,AL
	4975	ENDP		5051	SUB AH,AM
	4976	----		5052	RET
	4977	;		5053	MOTOR_ON ENDP
	4978	;		5054	;
	4979	;		5055	;
	4980	;		5056	;
	4981	;		5057	;
	4982	;		5058	;
	4983	;		5059	;
	4984	;		5060	IN AL,PORT_B
	4985	;		5061	OR AL,0BH
	4986	;		5062	JMP M3
	4987	;		5063	MOTOR_OFF ENDP
	4988	;		5064	;
	4989	;		5065	;
	4990	;		5066	;
	4991	;		5067	;
	4992	;		5068	;
	4993	;		5069	;
	4994	;		5070	;
	4995	;		5071	;
	4996	;		5072	;
	4997	;		5073	;
	4998	;		5074	;
	4999	;		5075	;
	5000	;		5076	;
	5001	;		5077	;
F659	5002	CASSETTE_IO PROC FAR		5078	;
F659 F8	5003	STI		5079	;
F65A 1E	5004	PUSH DS		5080	;
F65B 50	5005	PUSH AX		5081	;
F65C 8E4000	5006	MOV AX,DATA		5082	;
F65F 8E0B	5007	MOV DS,AX		5083	;
F661 02671007F	5008	AND 0105,BREAK_7FH		5084	;
F666 38	5009	POP AX		5085	;
F667 8E0400	5010	CALL M1		5086	;
F66A 1F	5011	POP DS		5087	;
F66B 1A0200	5012	RET 2		5088	;
F66E	5013	CASSETTE_IO ENDP		5089	;
	5014	M1 PROC NEAR		5090	;
	5015	;		5091	;
	5016	;		5092	;
	5017	;		5093	;
	5018	;		5094	;
	5019	;		5095	;
	5020	;		5096	;
	5021	;		5097	;
	5022	;		5098	;
	5023	;		5099	;
	5024	;		5100	;
	5025	;		5101	;
	5026	;		5102	;
	5027	;		5103	;
	5028	;		5104	;
	5029	;		5105	;
	5030	;		5106	;
	5031	;		5107	;
	5032	;		5108	;
	5033	;		5109	;
	5034	;		5110	;
	5035	;		5111	;
	5036	;		5112	;
	5037	;		5113	;
	5038	;		5114	;
	5039	;		5115	;
	5040	;		5116	;
	5041	;		5117	;
	5042	;			

LOC OBJ	LINE	SOURCE	LOC OBJ	LINE	SOURCE
P80A E304	5118	JCKZ M9	P936 7403	5194	JZ M17
P80C 718F	5119	JNC M4	P938 E962FF	5195	JMP M4
P80E E2E8	5120	LOOP M8	P938	5196	M17: NO DATA FROM CASSETTE ERROR, I.E. TIMEOUT
P80F	5121	W9:		5197	-----
P80G 72E6	5122	JC M6		5198	RESTORE REGS
	5123			5199	POP CX
	5124			5200	POP BX
	5125			5201	POP DX
	5126			5202	SUB DX,DX
	5127			5203	MOV AH,04H
	5128			5204	PUSH AX
	5129			5205	M18: IN AL, 021H
	5130			5206	AND AL, 0FFH-1
	5131			5207	OUT 021H, AL
	5132			5208	CALL MOTOR_OFF
	5133			5209	POP AX
	5134			5210	POP AX
	5135			5211	CMP AH,01H
	5136			5212	CMP
	5137			5213	REI
	5138			5214	ENDP
	5139			5215	READ_BLOCK
	5140			5216	READ_BYTE
	5141			5217	PROC NEAR
	5142			5218	TO READ A BYTE FROM CASSETTE
	5143			5219	ON EXIT REG AL CONTAINS READ DATA BYTE
	5144			5220	-----
	5145			5221	PUSH BX
	5146			5222	PUSH CX
	5147			5223	MOV CL,0H
	5148			5224	M19: SET BIT COUNTER FOR 8 BITS
	5149			5225	BYTE-LASH
	5150			5226	PUSH CX
	5151			5227	SAVE CX
	5152			5228	-----
	5153			5229	READ DATA BIT FROM CASSETTE
	5154			5230	CALL READ_HALF_BIT
	5155			5231	JCZ M21
	5156			5232	PUSH BX
	5157			5233	CALL READ_HALF_BIT
	5158			5234	POP AX
	5159			5235	JCZ M21
	5160			5236	IF CX=0 THEN TIMEOUT DUE TO
	5161			5237	NO DATA TRANSITIONS
	5162			5238	IF CARRY FOR ZERO BIT
	5163			5239	CMP BX,04F0H
	5164			5240	CMP
	5165			5241	SAVE CARRY IN AH
	5166			5242	LAHF
	5167			5243	POP CX
	5168			5244	-----
	5169			5245	IF MS BIT OF BYTE IS READ FIRST.
	5170			5246	IF CARRY IS SET IF ONE BIT
	5171			5247	IF REG CH IS SHIFTED LEFT WITH
	5172			5248	CARRY BEING INSERTED INTO LS
	5173			5249	1 BIT OF CH.
	5174			5250	AFTER ALL 8 BITS HAVE BEEN
	5175			5251	READ. THE MS BIT OF THE DATA BYTE
	5176			5252	WILL BE IN THE MS BIT OF REG CH
	5177			5253	ROTATE REG CH LEFT WITH CARRY TO
	5178			5254	LS BIT OF REG CH
	5179			5255	RESTORE CARRY FOR CIRC ROUTINE
	5180			5256	GENERATE CRC FOR BIT
	5181			5257	LOOP TILL ALL 8 BITS OF DATA
	5182			5258	ASSEMBLED IN REG CH
	5183			5259	1 BYTE,ASH
	5184			5260	RETURN DATA BYTE IN REG AL
	5185			5261	1 NO-BIT-EX
	5186			5262	RESTORE REGS CX,BX
	5187			5263	POP CX
	5188			5264	POP BX
	5189			5265	IF FINISHED
	5190			5266	1 NO-DATA
	5191			5267	RESTORE CX
	5192			5268	POP CX
	5193			5269	STC

LOC OBJ	LINE	SOURCE
F97E EBF9	5266	JMP W20 ; PD_BYTE_EX
	5269	READ_BYTE ENOP
	5270	-----
F980	5271	READ_HALF_BIT PROC NEAR
	5272	PURPOSE:
	5273	TO COMPUTE TIME TILL NEXT DATA
	5274	TRANSITION (EDGE)
	5275	ON ENTRY:
	5276	EDGE_CNT CONTAINS LAST EDGE COUNT
	5277	ON EXIT:
	5278	EDGE_CNT CONTAINS LAST EDGE COUNT
	5279	ON ENTRY:
	5280	AX CONTAINS OLD LAST EDGE COUNT
	5281	AX CONTAINS PULSE WIDTH (HALF BIT)
	5282	-----
F980 B9A400	5283	MOV CX, 100
F981 BAC2A000	5284	MOV AH, LAST_VAL
F982 E642	5285	M22:
F983 2410	5286	IN AL, PORT_C
F984 3AC4	5287	AND AL, 010H
F985 E1F6	5288	OR AL, 01H
F986 A26800	5289	LODPE M22
F987 8000	5290	MOV AL, 0
F988 E643	5291	OUT TIR_CTL, AL
F989 E440	5292	IN AL, TIR0
F98A 8AE0	5293	MOV AH, AL
F98B 1440	5294	IN AL, TIR0
F98C 8AC4	5295	XCHG AL, AH
F98D 0B16700	5296	MOV BX, EDGE_CNT
F98E 2B06	5297	SUB BX, AX
F98F A36700	5298	MOV EDGE_CNT, AX
F990 C3	5299	RET
	5300	-----
F991	5301	READ_HALF_BIT ENOP
F992	5302	WRITE_BLOCK PROC NEAR
	5303	-----
F993	5304	WRITE 1 OR MORE 256 BYTE BLOCKS TO CASSETTE.
	5305	THE DATA IS PADDED TO FILL OUT THE LAST 256 BYTE BLOCK.
	5306	ON ENTRY:
	5307	AX POINTS TO MEMORY BUFFER ADDRESS
	5308	CX CONTAINS NUMBER OF BYTES TO WRITE
	5309	-----
F994	5310	ON EXIT:
	5311	AX POINTS 1 BYTE PAST LAST BYTE WRITTEN TO CASSETTE
	5312	CX IS ZERO
	5313	-----
F995 53	5314	PUSH BX
F996 51	5315	IN AL, PORT_B
F997 E461	5316	AND AL, NOT 02H
F998 24F0	5317	OR AL, 01H
F999 0C01	5318	OUT PORT_B, AL
F99A E641	5319	MOV AL, 000H
F99B 0B06	5320	OUT TIR_CTL, AL
F99C E643	5321	CALL BEGIN_LOOP
F99D E64000	5322	MOV AX, 110H
F99E 0B0006	5323	CALL M31
F99F 800008	5324	MOV CX, 0000H
F9A0	5325	M23:
F9A1 F9	5326	STC
F9A2 E64000	5327	CALL WRITE_BYTE
F9A3 E2FA	5328	LOOP M23
F9A4 F6	5329	CLC
F9A5 E64200	5330	CALL WRITE_BYTE
F9A6 59	5331	POP CX
F9A7 5B	5332	POP BX
F9A8 8016	5333	MOV AL, 16H
F9A9 E64400	5334	CALL WRITE_BYTE
	5335	-----
	5336	WRITE 1 OR MORE 256 BYTE BLOCKS TO CASSETTE
	5337	ON ENTRY:
	5338	AX POINTS TO MEMORY BUFFER ADDRESS
	5339	CX CONTAINS NUMBER OF BYTES TO WRITE
	5340	-----
	5341	ON EXIT:
	5342	AX POINTS 1 BYTE PAST LAST BYTE WRITTEN TO CASSETTE
	5343	CX IS ZERO
	5344	-----
	5345	WRITE_BLOCK:
	5346	MOV CX, 256
	5347	M24:
	5348	MOV AL, 010H
	5349	CALL WRITE_BYTE
	5350	JCZ M25
	5351	INC BX
	5352	DEC BX
	5353	DEC BX
	5354	DEC BX
	5355	DEC BX
	5356	DEC BX
	5357	DEC BX
	5358	DEC BX
	5359	DEC BX
	5360	DEC BX
	5361	DEC BX
	5362	DEC BX
	5363	DEC BX
	5364	DEC BX
	5365	DEC BX
	5366	DEC BX
	5367	DEC BX
	5368	DEC BX
	5369	DEC BX
	5370	DEC BX
	5371	DEC BX
	5372	DEC BX
	5373	DEC BX
	5374	DEC BX
	5375	DEC BX
	5376	DEC BX
	5377	DEC BX
	5378	DEC BX
	5379	DEC BX
	5380	DEC BX
	5381	DEC BX
	5382	DEC BX
	5383	DEC BX
	5384	DEC BX
	5385	DEC BX
	5386	DEC BX
	5387	DEC BX
	5388	DEC BX
	5389	DEC BX
	5390	DEC BX
	5391	DEC BX
	5392	DEC BX
	5393	DEC BX
	5394	DEC BX
	5395	DEC BX
	5396	DEC BX
	5397	DEC BX
	5398	DEC BX
	5399	DEC BX
	5400	DEC BX
	5401	DEC BX
	5402	DEC BX
	5403	DEC BX
	5404	DEC BX
	5405	DEC BX
	5406	DEC BX
	5407	DEC BX
	5408	DEC BX
	5409	DEC BX
	5410	DEC BX
	5411	DEC BX
	5412	DEC BX
	5413	DEC BX
	5414	DEC BX

[illegible]

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[illegible]

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LOG OBJ          LINE      SOURCE
FEB0 6336600018  R 5715 CMP     TIMER_HIGH_010H : TEST FOR COUNT EQUALLING 24 HOURS
FEB0 7519        R 5716 JNZ     T5           : DISKETTE_CTL
FEBF 8136C00000  R 5717 CMP     TIMER_LOW_080H : DISKETTE_CTL
FEC5 7511        R 5718 JNZ     T5
5719             J----- TIMER HAS GONE 24 HOURS
5720             MOV     TIMER_HIGH_0
5721             MOV     TIMER_LOW_0
5722             MOV     TIMER_OFF_1
5723             MOV     TIMER_OFF_1
5724             MOV     TIMER_OFF_1
5725             J----- TEST FOR DISKETTE TIME OUT
5726             J-----
5727             TS:
5728             DEC     MOTOR_COUNT
5729             JNZ     T6
5730             JNZ     MOTOR_STATUS_0F0H : RETURN IF COUNT NOT OUT
5731             JNZ     T6
5732             MOV     MOTOR_STATUS_0F0H : TURN OFF MOTOR RUNNING BITS
5733             MOV     DX_03F2H : IDC CTL PORT
5734             OUT     DX_03F2H : TURN OFF THE MOTOR
5735             J-----
5736             T6:
5737             INT     1CH
5738             MOV     AL_EDI
5739             OUT     020H:AL
5740             POP     DX
5741             POP     AX
5742             POP     DS
5743             JRET
5744             ENOP
5745             J-----
5746             ; THESE ARE THE VECTORS WHICH ARE MOVED INTO
5747             ; THE 8086 INTERRUPT AREA DURING POWER ON
5748             J-----
5749             VECTOR_TABLE LABEL WORD : VECTOR TABLE FOR MOVIE TO INTERRUPTS
5750
5751             DM      OFFSET TIMER_INT : INTERRUPT 0
5752             DM      CODE
5753
5754             DM      OFFSET K8_INT : INTERRUPT 9
5755             DM      CODE
5756
5757             DD      0
5758             DD      0
5759             DD      0
5760             DD      0
5761             DD      0
5762             DD      0
5763             DD      0
5764             DD      0
5765             DD      0
5766             DD      0
5767             DD      0
5768             DD      0
5769             DD      0
5770             DD      0
5771             DD      0
5772             DD      0
5773             DD      0
5774             DD      0
5775             DD      0
5776             DD      0
5777             DD      0
5778             DD      0
5779             DD      0
5780             DD      0
5781             DD      0
5782             DD      0
5783             DD      0
5784             DD      0
5785             DD      0
5786             DD      0
5787             DD      0
5788             DD      0
5789             DD      0
5790             DD      0

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LOG OBJ          LINE      SOURCE
F733 0000        DM 5791 DM      00000H : INTERRUPT 10H
F735 0076        DM 5792 DM      0F400H : ROM BASIC ENTRY POINT
5793             R
5794             R
5795             R
5796             R
5797             R
5798             R
5799             R
5800             R
5801             R
5802             R
5803             R
5804             R
5805             R
5806             R
5807             R
5808             R
5809             R
5810             R
5811             R
5812             R
5813             R
5814             R
5815             R
5816             R
5817             R
5818             R
5819             R
5820             R
5821             R
5822             R
5823             R
5824             R
5825             R
5826             R
5827             R
5828             R
5829             R
5830             R
5831             R
5832             R
5833             R
5834             R
5835             R
5836             R
5837             R
5838             R
5839             R
5840             R
5841             R
5842             R
5843             R
5844             R
5845             R
5846             R
5847             R
5848             R
5849             R
5850             R
5851             R
5852             R
5853             R
5854             R
5855             R
5856             R
5857             R
5858             R
5859             R
5860             R
5861             R
5862             R
5863             R
5864             R
5865             R

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Notes for the BIOS Listing

1. The wait loop for the printer times out on form feed of > 51 lines. — line ref (3069)
2. Mode controls for the 320 x 200 video have Color/BW reversed. — line ref (3338)
3. The RS232 Timeout is 80 decimal, not 80 hexadecimal. — line ref (1566)
4. The Base Pointer register is destroyed by some video calls.
5. D,04 character in the character generator has 08 as its last value, S/80. — line ref (511)
6. If you hit print screen in the Color/Graphics 80x25 Character Mode, the screen may not display during the print cycle.

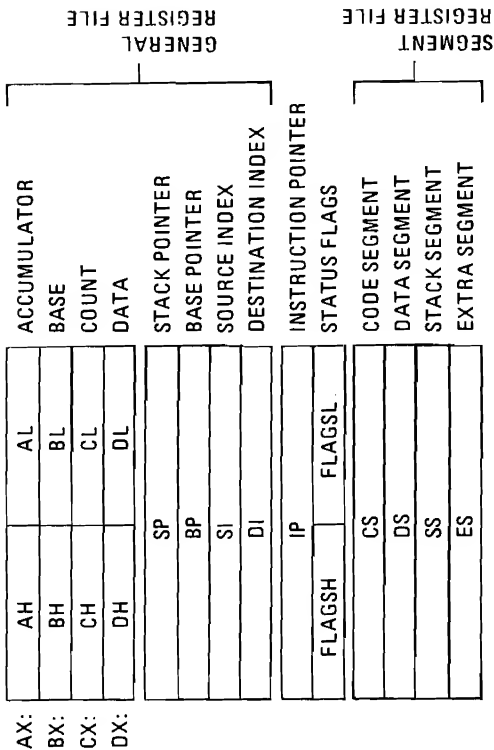
LOC OBJ	LINE	SOURCE
	5865	*****
	5867	! THE LOOP FROM PRI10 TO THE INSTRUCTION PRIOR TO PRI20
	5868	! IS THE LOOP TO READ EACH CURSOR POSITION FROM THE SCREEN
	5869	! AND PRINT.
	5870	*****
FF7F B402	5871	PRI10: MOV AH,2 ;TO INDICATE CURSOR SET REQUEST
FF81 C010	5872	INT 10H ;HEM CURSOR POSITION ESTABLISHED
FF83 B408	5873	MOV AH,0 ;TO INDICATE READ CHARACTER
FF85 C010	5874	INT 10H ;CHARACTER NOW IN AL
FF87 A0C0	5875	OR AL,AL ;SEE IF VALID CHAR
FF89 3502	5876	JNZ PRI15 ;JUMP IF VALID CHAR
FF8B B020	5877	MOV AL,' ' ;MAKE A BLANK
FF8D	5878	
FF8F 52	5879	PRI15: PUSH DX ;SAVE CURSOR POSITION
FF91 3302	5880	XOR DX,DX ;INDICATE PRINTER 1
FF93 32E4	5881	XOR AH,AH ;TO INDICATE PRINT CHAR IN (AL)
FF95 C017	5882	INT 17H ;PRINT THE CHARACTER
FF97 5A	5883	POP DX ;RECALL CURSOR POSITION
FF99 34C25	5884	TEST AH,25H ;TEST FOR PRINTER ERROR
FF9B 7521	5885	JNZ ERR10 ;JUMP IF ERROR DETECTED
FF9D EC2	5886	INC DL ;ADVANCE TO NEXT COLUMN
FF9F 34C4	5887	CHP CL,DL ;SEE IF AT END OF LINE
FFA1 320F	5888	JNZ PRI10 ;IF NOT PROCEED
FFA3 3202	5889	XOR DX,DX ;BACK TO COLUMN 0
FFA5 84E2	5890	MOV AH,DL ;AH:=0
FFA7 52	5891	PUSH DX ;SAVE NEW CURSOR POSITION
FFA9 E0300	5892	CALL CRLF ;LINK FEED CARRIAGE RETURN
FFAB 5A	5893	POP DX ;RECALL CURSOR POSITION
FFAD EC6	5894	INC CH,CH ;ADVANCE TO NEXT LINE
FFAF 7500	5895	CHP CH,CH ;FINISHED?
FFB1 5A	5896	JNZ PRI10 ;IF NOT CONTINUE
FFB3 5A	5897	POP DX ;RECALL CURSOR POSITION
FFB5 8402	5898	MOV AH,2 ;TO INDICATE CURSOR SET REQUEST
FFB7 C010	5899	INT 10H ;CURSOR POSITION RESTORED
FFB9 C0A000000	5900	MOV STATUS_BYTE,0 ;INDICATE FINISHED
FFBB E00A	5901	JMP SHORT EXIT ;EXIT THE ROUTINE
FFBD 5A	5902	POP DX ;GET CURSOR POSITION
FFBF B402	5903	MOV AH,2 ;TO REQUEST CURSOR SET
FFC1 C010	5904	INT 10H ;CURSOR POSITION RESTORED
FFC3 C0A0000FF	5905	MOV STATUS_BYTE,0FFH ;INDICATE ERROR
	5906	
FFC5 5A	5907	POP DX ;PRESTORE ALL THE REGISTERS USED
FFC7 59	5908	POP CX
FFC9 5B	5909	POP BX
FFCB 5A	5910	POP AX
FFCD 1F	5911	POP DS
FFCF CF	5912	IRET
	5913	PRINT_SCREEN END
	5914	
	5915	!----- CARRIAGE RETURN, LINE FEED SUBROUTINE
	5916	
FFD1	5917	CRLF PROC NEAR
FFD3 3302	5918	XOR DX,DX
FFD5 32E4	5919	XOR AH,AH ;WELL NOW SEND INITIAL LF,CR TO PRINTER
FFD7 B00A	5920	MOV AL,120H ;LF
FFD9 C017	5921	INT 17H ;SEND THE LINE FEED
FFDB 32E4	5922	XOR AH,AH ;NOW FOR THE CR
FFDD B000	5923	MOV AL,150H ;CR
FFDF C017	5924	INT 17H ;SEND THE CARRIAGE RETURN
FFE1 C3	5925	RET
	5926	CRLF END
	5927	CODE ENDS
	5928	
	5929	!-----
	5930	! POWER ON RESET VECTOR
FFFF	5931	VECTOR SEGMENT AT 0FFFFH
	5932	
	5933	!----- POWER ON RESET
0000 E450000F0	5934	JMP RESET
	5935	
	5936	DB '04/24/81' ; RELEASE MARKER
0005 30342F32342F30	5937	
	5938	VECTOR ENDS
	5939	END
	5940	

NOTES

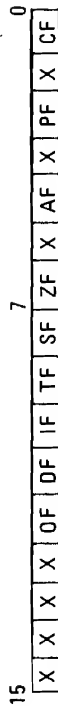
APPENDIX B. ASSEMBLY INSTRUCTION SET REFERENCE

APPENDIX B

8088 REGISTER MODEL



Instructions which reference the flag register file as a 16-bit object use the symbol **FLAGS** to represent the file:



X = Don't Care

- 8080 FLAGS:**
 - AF: AUXILIARY CARRY - BCD
 - CF: CARRY FLAG
 - PF: PARITY FLAG
 - SF: SIGN FLAG
 - ZF: ZERO FLAG
- 8088 FLAGS:**
 - DF: DIRECTION FLAG (STRINGS)
 - IF: INTERRUPT ENABLE FLAG
 - OF: OVERFLOW FLAG (CF ⊕ SF)
 - TF: TRAP - SINGLE STEP FLAG

OPERAND SUMMARY

"reg" field Bit Assignments:

16-Bit (w=1)	8-Bit (w=0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

SECOND INSTRUCTION BYTE SUMMARY

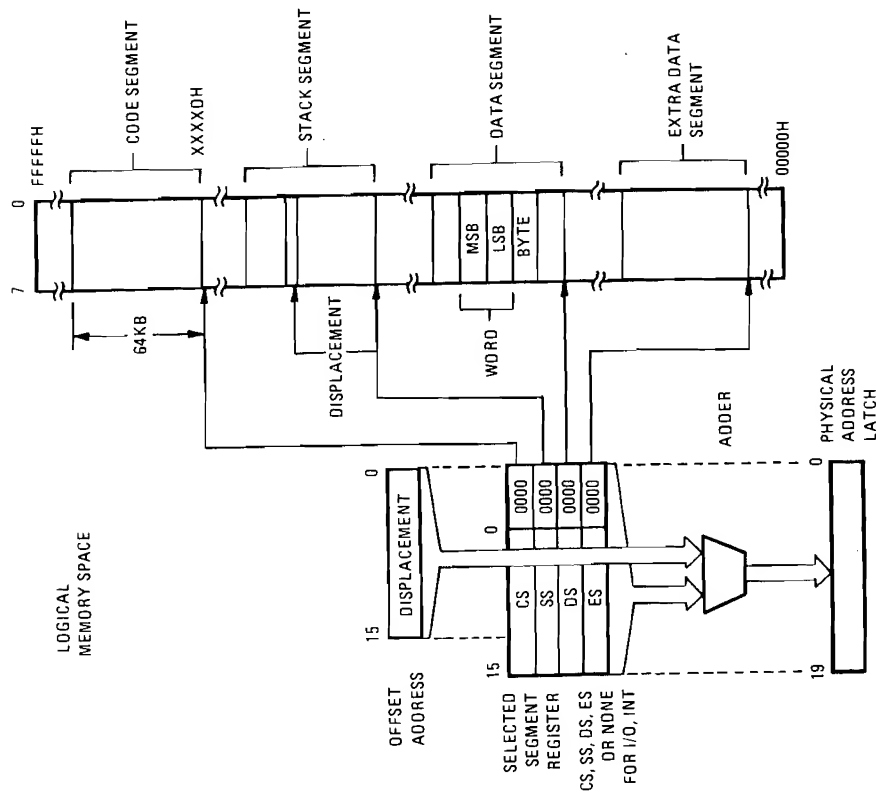
mod	xxx	r/m
-----	-----	-----

mod	Displacement
00	DISP = 0*, disp-low and disp-high are absent
01	DISP = disp-low sign-extended to 16-bits, disp-high is absent
10	DISP = disp-high: disp-low
11	r/m is treated as a "reg" field

r/m	Operand Address
000	(BX) + (SI) + DISP
001	(BX) + (DI) + DISP
010	(BP) + (SI) + DISP
011	(BP) + (DI) + DISP
100	(SI) + DISP
101	(DI) + DISP
110	(BP) + DISP*
111	(BX) + DISP

DISP follows 2nd byte of instruction (before data if required).
*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

MEMORY SEGMENTATION MODEL



SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

USE OF SEGMENT OVERRIDE

OPERAND REGISTER	DEFAULT	WITH OVERRIDE PREFIX
IP (code address)	CS	Never
SP (stack address)	SS	Never
BP (stack address or stack marker)	SS	BP + DS or ES, or CS
SI or DI (not incl. strings)	DS	ES, SS, or CS
SI (implicit source addr for strings)	DS	ES, SS, or CS
DI (implicit dest addr for strings)	ES	Never

DATA TRANSFER

MOV = Move

Register/memory to/ from register

1 0 0 0 1 0 d w mod reg r/m

Immediate to register/memory

1 1 0 0 0 1 1 w mod 0 0 0 r/m data data if w=1

Immediate to register

1 0 1 1 w reg data data if w=1

Memory to accumulator

1 0 1 0 0 0 0 w addr-low addr-high

Accumulator to memory

1 0 1 0 0 0 1 w addr-low addr-high

Register/memory to segment register

1 0 0 0 1 1 1 0 mod 0 reg r/m

Segment register to register/memory

1 0 0 0 1 1 0 0 mod 0 reg r/m

PUSH = Push

Register/memory

1 1 1 1 1 1 1 1 mod 1 1 0 r/m

Register

0 1 0 1 0 reg

Segment register

0 0 0 reg 1 1 0

POP = Pop

Register/memory

1 0 0 0 1 1 1 1 mod 0 0 0 r/m

Register

0 1 0 1 1 reg

Segment register

0 0 0 reg 1 1 1

XCHG = Exchange

Register/memory with register

1	0	0	0	1	1	w	mod	reg	r/m
---	---	---	---	---	---	---	-----	-----	-----

Register with accumulator

1	0	0	1	0	reg
---	---	---	---	---	-----

IN = Input to AL/AX from

Fixed port

1	1	1	0	0	1	0	w	port
---	---	---	---	---	---	---	---	------

Variable port (DX)

1	1	1	0	1	1	0	w
---	---	---	---	---	---	---	---

OUT = Output from AL/AX to

Fixed port

1	1	1	0	0	1	1	w	port
---	---	---	---	---	---	---	---	------

Variable port (DX)

1	1	1	0	1	1	1	w
---	---	---	---	---	---	---	---

XLAT = Translate byte to AL

1	1	0	1	0	1	1	1
---	---	---	---	---	---	---	---

LEA = Load EA to register

1	0	0	0	1	1	0	1	mod	reg	r/m
---	---	---	---	---	---	---	---	-----	-----	-----

LDS = Load pointer to DS

1	1	0	0	0	1	0	1	mod	reg	r/m
---	---	---	---	---	---	---	---	-----	-----	-----

LES = Load pointer to ES

1	1	0	0	0	1	0	0	mod	reg	r/m
---	---	---	---	---	---	---	---	-----	-----	-----

LAHF = Load AH with flags

1	0	0	1	1	1	1	1
---	---	---	---	---	---	---	---

SAHF = Store AH into flags

1	0	0	1	1	1	1	0
---	---	---	---	---	---	---	---

PUSHF = Push flags

1	0	0	1	1	1	0	0
---	---	---	---	---	---	---	---

POPF = Pop flags

1	0	0	1	1	1	0	1
---	---	---	---	---	---	---	---

ARITHMETIC**ADD** = Add

Reg./memory with register to either

0	0	0	0	0	d	w	mod	reg	r/m
---	---	---	---	---	---	---	-----	-----	-----

Immediate to register/memory

1	0	0	0	0	s	w	mod	0	0	0	r/m	data	data if s:w=01
---	---	---	---	---	---	---	-----	---	---	---	-----	------	----------------

Immediate to accumulator

0	0	0	0	0	1	0	w	data	data if w=1
---	---	---	---	---	---	---	---	------	-------------

ADC = Add with carry

Reg./memory with register to either

0	0	0	1	0	0	d	w	mod	reg	r/m
---	---	---	---	---	---	---	---	-----	-----	-----

Immediate to register/memory

1	0	0	0	0	s	w	mod	0	1	0	r/m	data	data if s:w=01
---	---	---	---	---	---	---	-----	---	---	---	-----	------	----------------

Immediate to accumulator

0	0	0	1	0	1	0	w	data	data if w=1
---	---	---	---	---	---	---	---	------	-------------

INC = Increment

Register/memory

1	1	1	1	1	1	1	w	mod	0	0	0	r/m
---	---	---	---	---	---	---	---	-----	---	---	---	-----

Register

0	1	0	0	0	reg
---	---	---	---	---	-----

AAA = ASCII adjust for add

0	0	1	1	0	1	1	1
---	---	---	---	---	---	---	---

DAA = Decimal adjust for add

0	0	1	0	0	1	1	1
---	---	---	---	---	---	---	---

SUB = Subtract

Reg./memory and register to either

0	0	1	0	1	0	d	w	mod	reg	r/m
---	---	---	---	---	---	---	---	-----	-----	-----

Immediate from register/memory

1	0	0	0	0	s	w	mod	1	0	1	r/m	data	data if s:w=01
---	---	---	---	---	---	---	-----	---	---	---	-----	------	----------------

Immediate from accumulator

0	0	1	0	1	1	0	w	data	data if w=1
---	---	---	---	---	---	---	---	------	-------------

SBB = Subtract with borrow

Reg./memory and register to either

0	0	0	1	1	0	d	w	mod	reg	r/m
---	---	---	---	---	---	---	---	-----	-----	-----

Immediate from register/memory

1	0	0	0	0	s	w	mod	0	1	1	r/m	data	data if s:w=01
---	---	---	---	---	---	---	-----	---	---	---	-----	------	----------------

Immediate from accumulator

0	0	0	1	1	0	w	data	data if w=1
---	---	---	---	---	---	---	------	-------------

DEC = Decrement

Register/memory

1	1	1	1	1	1	w	mod	0	0	1	r/m
---	---	---	---	---	---	---	-----	---	---	---	-----

Register

0	1	0	0	1	reg
---	---	---	---	---	-----

NEG = Change sign

1	1	1	0	1	1	w	mod	0	1	1	r/m
---	---	---	---	---	---	---	-----	---	---	---	-----

CMP = Compare

Register/memory and register

0	0	1	1	0	d	w	mod	reg	r/m
---	---	---	---	---	---	---	-----	-----	-----

Immediate with register/memory

1	0	0	0	0	s	w	mod	1	1	1	r/m	data	data if s:w=01
---	---	---	---	---	---	---	-----	---	---	---	-----	------	----------------

Immediate with accumulator

0	0	1	1	1	0	w	data	data if w=1
---	---	---	---	---	---	---	------	-------------

AAS = ASCII adjust for subtract

0	0	1	1	1	1	1
---	---	---	---	---	---	---

DAS = Decimal adjust for subtract

0	0	1	0	1	1	1
---	---	---	---	---	---	---

MUL = Multiply (unsigned)

1	1	1	0	1	1	w	mod	1	0	0	r/m
---	---	---	---	---	---	---	-----	---	---	---	-----

IMUL = Integer multiply (signed)

1	1	1	0	1	1	w	mod	1	0	1	r/m
---	---	---	---	---	---	---	-----	---	---	---	-----

AAM = ASCII adjust for multiply

1	1	0	1	0	1	0	0	0	0	0	1	0
---	---	---	---	---	---	---	---	---	---	---	---	---

DIV = Divide (unsigned)

1	1	1	0	1	1	w	mod	1	1	0	r/m
---	---	---	---	---	---	---	-----	---	---	---	-----

IDIV = Integer divide (signed)

1	1	1	0	1	1	w	mod	1	1	1	r/m
---	---	---	---	---	---	---	-----	---	---	---	-----

AAD = ASCII adjust for divide

1	1	0	1	0	1	0	1	0	0	0	1	0
---	---	---	---	---	---	---	---	---	---	---	---	---

CBW = Convert byte to word

1	0	0	1	1	0	0
---	---	---	---	---	---	---

CWD = Convert word to double word

1	0	0	1	1	0	0	1
---	---	---	---	---	---	---	---

LOGIC

NOT = Invert

1	1	1	0	1	1	w	mod	0	1	0	r/m
---	---	---	---	---	---	---	-----	---	---	---	-----

SHL/SAL = Shift logical/arithmetic left

1	1	0	1	0	0	v	w	mod	1	0	0	r/m
---	---	---	---	---	---	---	---	-----	---	---	---	-----

SHR = Shift logical right

1	1	0	1	0	0	v	w	mod	1	0	1	r/m
---	---	---	---	---	---	---	---	-----	---	---	---	-----

SAR = Shift arithmetic right

1	1	0	1	0	0	v	w	mod	1	1	1	r/m
---	---	---	---	---	---	---	---	-----	---	---	---	-----

ROL = Rotate left

1	1	0	1	0	0	v	w	mod	0	0	0	r/m
---	---	---	---	---	---	---	---	-----	---	---	---	-----

ROR = Rotate right

1	1	0	1	0	0	v	w	mod	0	0	1	r/m
---	---	---	---	---	---	---	---	-----	---	---	---	-----

RCL = Rotate through carry left

1	1	0	1	0	0	v	w	mod	0	1	0	r/m
---	---	---	---	---	---	---	---	-----	---	---	---	-----

RCR = Rotate through carry right

1	1	0	1	0	0	v	w	mod	0	1	1	r/m
---	---	---	---	---	---	---	---	-----	---	---	---	-----

AND = And

Reg./memory and register to either

0	0	1	0	0	d	w	mod	reg	r/m
---	---	---	---	---	---	---	-----	-----	-----

Immediate to register/memory

1	0	0	0	0	0	w	mod	1	0	0	r/m	data	data if w=1
---	---	---	---	---	---	---	-----	---	---	---	-----	------	-------------

Immediate to accumulator

0	0	1	0	0	1	0	w	data	data if w=1
---	---	---	---	---	---	---	---	------	-------------

TEST = And function to flags, no result

Register/memory and register

1	0	0	0	1	0	w	mod	reg	r/m
---	---	---	---	---	---	---	-----	-----	-----

Immediate data and register/memory

1	1	1	1	0	1	1	w	mod	0	0	0	r/m	data	data if w=1
---	---	---	---	---	---	---	---	-----	---	---	---	-----	------	-------------

Immediate data and accumulator

1	0	1	0	1	0	0	w	data	data if w=1
---	---	---	---	---	---	---	---	------	-------------

OR = Or

Reg./memory and register to either

0	0	0	1	0	d	w	mod	reg	r/m
---	---	---	---	---	---	---	-----	-----	-----

Immediate to register/memory

1	0	0	0	0	0	w	mod	0	0	1	r/m	data	data if w=1
---	---	---	---	---	---	---	-----	---	---	---	-----	------	-------------

Immediate to accumulator

0	0	0	1	1	0	w	data	data if w=1
---	---	---	---	---	---	---	------	-------------

XOR = Exclusive or

Reg./memory and register to either

0	0	1	1	0	d	w	mod	reg	r/m
---	---	---	---	---	---	---	-----	-----	-----

Immediate to register/memory

1	0	0	0	0	0	w	mod	1	1	0	r/m	data	data if w=1
---	---	---	---	---	---	---	-----	---	---	---	-----	------	-------------

Immediate to accumulator

0	0	1	1	0	1	0	w	data	data if w=1
---	---	---	---	---	---	---	---	------	-------------

STRING MANIPULATION**REP = Repeat**

1	1	1	1	0	0	1	z
---	---	---	---	---	---	---	---

MOVS = Move String

1	0	1	0	0	1	0	w
---	---	---	---	---	---	---	---

CMPS = Compare String

1	0	1	0	0	1	1	w
---	---	---	---	---	---	---	---

SCAS = Scan String

1	0	1	0	1	1	1	w
---	---	---	---	---	---	---	---

LDS = Load String

1	0	1	0	1	1	0	w
---	---	---	---	---	---	---	---

STOS = Store String

1	0	1	0	1	0	1	w
---	---	---	---	---	---	---	---

CONTROL TRANSFER**CALL = Call**

Direct within segment

1	1	1	0	1	0	0	0	disp-low	disp-high
---	---	---	---	---	---	---	---	----------	-----------

Indirect within segment

1	1	1	1	1	1	1	mod	0	1	0	r/m
---	---	---	---	---	---	---	-----	---	---	---	-----

Direct intersegment

1	0	0	1	1	0	1	0	offset-low	offset-high
								seg-low	seg-high

Indirect intersegment

1	1	1	1	1	1	1	mod	0	1	1	r/m
---	---	---	---	---	---	---	-----	---	---	---	-----

JMP = Unconditional Jump

Direct within segment

1	1	1	0	1	0	0	1	disp-low	disp-high
---	---	---	---	---	---	---	---	----------	-----------

Direct within segment-short

1	1	1	0	1	0	1	disp
---	---	---	---	---	---	---	------

Indirect within segment

1	1	1	1	1	1	1	mod	1	0	0	r/m
---	---	---	---	---	---	---	-----	---	---	---	-----

Direct intersegment

1	1	1	0	1	0	1	0	offset-low		offset-high
								seg-low		seg-high

Indirect intersegment

1	1	1	1	1	1	1	mod	1	0	1	r/m
---	---	---	---	---	---	---	-----	---	---	---	-----

RET = Return from CALL

Within segment

1	1	0	0	0	1	1
---	---	---	---	---	---	---

Within seg. adding immed to SP

1	1	0	0	0	1	0	data-low		data-high
---	---	---	---	---	---	---	----------	--	-----------

Intersegment

1	1	0	0	1	0	1	1
---	---	---	---	---	---	---	---

Intersegment, adding immediate to SP

1	1	0	0	1	0	1	0	data-low		data-high
---	---	---	---	---	---	---	---	----------	--	-----------

JE/JZ = Jump on equal/zero

0	1	1	0	1	0	0	disp
---	---	---	---	---	---	---	------

JL/JNGE = Jump on less/not greater or equal

0	1	1	1	1	0	0	disp
---	---	---	---	---	---	---	------

JLE/JNG = Jump on less or equal/not greater

0	1	1	1	1	1	0	disp
---	---	---	---	---	---	---	------

JB/JNAE = Jump on below/not above or equal

0	1	1	1	0	0	1	0	disp
---	---	---	---	---	---	---	---	------

JBE/JNA = Jump on below or equal/not above

0	1	1	1	0	1	1	0	disp
---	---	---	---	---	---	---	---	------

JP/JPE = Jump on parity/parity even

0	1	1	1	0	1	0	disp
---	---	---	---	---	---	---	------

JO = Jump on overflow

0	1	1	1	0	0	0	disp
---	---	---	---	---	---	---	------

JS = Jump on sign

0	1	1	1	0	0	0	disp
---	---	---	---	---	---	---	------

JNE/JNZ = Jump on not equal/not zero

0	1	1	0	1	0	1	disp
---	---	---	---	---	---	---	------

JNL/JGE = Jump on not less/greater or equal

0	1	1	1	1	0	1	disp
---	---	---	---	---	---	---	------

JNLE/JG = Jump on not less or equal/greater

0	1	1	1	1	1	1	disp
---	---	---	---	---	---	---	------

JNB/JAE = Jump on not below/above or equal

0	1	1	1	0	0	1	disp
---	---	---	---	---	---	---	------

JNBE/JA = Jump on not below or equal/above

0	1	1	1	0	1	1	disp
---	---	---	---	---	---	---	------

JNP/JPO = Jump on not parity/parity odd

0	1	1	1	0	1	1	disp
---	---	---	---	---	---	---	------

JNO = Jump on not overflow

0	1	1	1	0	0	1	disp
---	---	---	---	---	---	---	------

JNS = Jump on not sign

0	1	1	1	0	0	1	disp
---	---	---	---	---	---	---	------

LOOP = Loop CX times

1	1	1	0	0	1	0	disp
---	---	---	---	---	---	---	------

LOOPZ/LOOPE = Loop while zero/equal

1	1	1	0	0	0	1	disp
---	---	---	---	---	---	---	------

LOOPNZ/LOOPE = Loop while not zero/not equal

1	1	1	0	0	0	0	disp
---	---	---	---	---	---	---	------

JCXZ = Jump on CX zero

1	1	1	0	0	1	1	disp
---	---	---	---	---	---	---	------

8088 CONDITIONAL TRANSFER OPERATIONS

Instruction	Condition	Interpretation
JE or JZ	ZF = 1	"equal" or "zero"
JL or JNGE	(SF xor OF) = 1	"less" or "not greater or equal"
JLE or JNG	((SF xor OF) or ZF) = 1	"less or equal" or "not greater"
JB or JNAE	CF = 1	"below" or "not above or equal"
JBE or JNA	(CF or ZF) = 1	"below or equal" or "not above"
JP or JPE	PF = 1	"parity" or "parity even"
JO	OF = 1	"overflow"
JS	SF = 1	"sign"
JNE or JNZ	ZF = 0	"not equal" or "not zero"
JNL or JGE	(SF xor OF) = 0	"not less" or "greater or equal"
JNLE or JG	((SF xor OF) or ZF) = 0	"not less or equal" or "greater"
JNB or JAE	CF = 0	"not below" or "above or equal"
JNBE or JA	(CF or ZF) = 0	"not below or equal" or "above"
JNP or JPO	PF = 0	"not parity" or "parity odd"
JNO	OF = 0	"not overflow"
JNS	SF = 0	"not sign"

**"Above" and "below" refer to the relation between two unsigned values, while "greater" and "less" refer to the relation between two signed values.

INT = Interrupt

Type specified

1	1	0	0	1	1	0	1	type
---	---	---	---	---	---	---	---	------

Type 3

1	1	0	0	1	1	0	1
---	---	---	---	---	---	---	---

INTO = Interrupt on overflow

1	1	0	0	1	1	1	0
---	---	---	---	---	---	---	---

IRET = Interrupt return

1	1	0	0	1	1	1	1
---	---	---	---	---	---	---	---

PROCESSOR CONTROL

CLC = Clear carry

1	1	1	1	1	1	0	0	0
---	---	---	---	---	---	---	---	---

STC = Set carry

1	1	1	1	1	0	0	1
---	---	---	---	---	---	---	---

CMC = Complement carry

1	1	1	1	0	1	0	1
---	---	---	---	---	---	---	---

NOP = No operation

1	0	0	1	0	0	0	0
---	---	---	---	---	---	---	---

CLD = Clear direction

1	1	1	1	1	0	0
---	---	---	---	---	---	---

STD = Set direction

1	1	1	1	1	0	1
---	---	---	---	---	---	---

CLI = Clear interrupt

1	1	1	1	1	0	1	0
---	---	---	---	---	---	---	---

STI = Set interrupt

1	1	1	1	1	0	1	1
---	---	---	---	---	---	---	---

HLT = Halt

1	1	1	1	0	1	0	0
---	---	---	---	---	---	---	---

WAIT = Wait

1	0	0	1	1	0	1	1
---	---	---	---	---	---	---	---

LOCK = Bus lock prefix

1	1	1	1	0	0	0	0
---	---	---	---	---	---	---	---

ESC = Escape (to external device)

1	1	0	1	1	x	x	x	mod	x	x	x	r/m
---	---	---	---	---	---	---	---	-----	---	---	---	-----

Footnotes:

if d = 1 then "to"; if d = 0 then "from"

if w = 1 then word instruction; if w = 0 then byte instruction

if s:w = 01 then 16 bits of immediate data from the operand

if s:w = 11 then an immediate data byte is sign extended to form the

16-bit operand

if v = 0 then "count" = 1; if v = 1 then "count" in (CL)

x = don't care

z is used for some string primitives to compare with ZF FLAG

AL = 8-bit accumulator

AX = 16-bit accumulator

CX = Count register

DS = Data segment

DX = Variable port register

ES = Extra segment

Above/below refers to unsigned value

Greater = more positive;

Less = less positive (more negative) signed values

8088 INSTRUCTION SET MATRIX

HI	LO																
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	ADD	ADD	ADD	ADD	ADD	ADD	ADD	ADD	POP	ADD	ADD	ADD	ADD	ADD	ADD	ADD	ADD
1	ADC	ADC	ADC	ADC	ADC	ADC	ADC	ADC	POP	ADC	ADC	ADC	ADC	ADC	ADC	ADC	ADC
2	AND	AND	AND	AND	AND	AND	AND	AND	SS	AND	AND	AND	AND	AND	AND	AND	AND
3	XOR	XOR	XOR	XOR	XOR	XOR	XOR	XOR	SEG	XOR	XOR	XOR	XOR	XOR	XOR	XOR	XOR
4	INC	INC	INC	INC	INC	INC	INC	INC	SS	INC	INC	INC	INC	INC	INC	INC	INC
5	PUSH	PUSH	PUSH	PUSH	PUSH	PUSH	PUSH	PUSH	DI	PUSH	PUSH	PUSH	PUSH	PUSH	PUSH	PUSH	PUSH
6	AX	AX	AX	AX	AX	AX	AX	AX	DI	AX	AX	AX	AX	AX	AX	AX	AX
7	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0
8	Immed	Immed	Immed	Immed	Immed	Immed	Immed	Immed	XCHG	Immed	Immed	Immed	Immed	Immed	Immed	Immed	Immed
9	NOP	XCHG	XCHG	XCHG	XCHG	XCHG	XCHG	XCHG	XCHG	XCHG	XCHG	XCHG	XCHG	XCHG	XCHG	XCHG	XCHG
A	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	CMPS	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV
B	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV
C	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV
D	Shift	Shift	Shift	Shift	Shift	Shift	Shift	Shift	XLAT	Shift	Shift	Shift	Shift	Shift	Shift	Shift	Shift
E	LOOPNZ/	LOOPNZ/	LOOPNZ/	LOOPNZ/	LOOPNZ/	LOOPNZ/	LOOPNZ/	LOOPNZ/	OUT	LOOPNZ/	LOOPNZ/	LOOPNZ/	LOOPNZ/	LOOPNZ/	LOOPNZ/	LOOPNZ/	LOOPNZ/
F	LOCK	LOCK	LOCK	LOCK	LOCK	LOCK	LOCK	LOCK	Grp 1	LOCK	LOCK	LOCK	LOCK	LOCK	LOCK	LOCK	LOCK

b = byte operation
 d = direct
 f = from CPU reg
 i = immediate
 ia = immmed. to accum.
 id = indirect
 is = immmed. byte, sign ext.
 l = long ie. intersegment
 m = memory
 r/m = EA is second byte
 si = short intrasegment
 sr = segment register
 t = to CPU reg
 v = variable
 w = word operation
 z = zero

8088 INSTRUCTION SET MATRIX

HI	LO																
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	OR	OR	OR	OR	OR	OR	OR	OR	OR	OR	OR	OR	OR	OR	OR	OR	OR
1	SBB	SBB	SBB	SBB	SBB	SBB	SBB	SBB	SBB	SBB	SBB	SBB	SBB	SBB	SBB	SBB	SBB
2	SUB	SUB	SUB	SUB	SUB	SUB	SUB	SUB	SUB	SUB	SUB	SUB	SUB	SUB	SUB	SUB	SUB
3	CMP	CMP	CMP	CMP	CMP	CMP	CMP	CMP	CMP	CMP	CMP	CMP	CMP	CMP	CMP	CMP	CMP
4	DEC	DEC	DEC	DEC	DEC	DEC	DEC	DEC	DEC	DEC	DEC	DEC	DEC	DEC	DEC	DEC	DEC
5	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP
6	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX
7	JS	JS	JS	JS	JS	JS	JS	JS	JS	JS	JS	JS	JS	JS	JS	JS	JS
8	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV
9	CBW	CBW	CBW	CBW	CBW	CBW	CBW	CBW	CBW	CBW	CBW	CBW	CBW	CBW	CBW	CBW	CBW
A	TEST	TEST	TEST	TEST	TEST	TEST	TEST	TEST	TEST	TEST	TEST	TEST	TEST	TEST	TEST	TEST	TEST
B	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV	MOV
C	RET	RET	RET	RET	RET	RET	RET	RET	RET	RET	RET	RET	RET	RET	RET	RET	RET
D	ESC	ESC	ESC	ESC	ESC	ESC	ESC	ESC	ESC	ESC	ESC	ESC	ESC	ESC	ESC	ESC	ESC
E	CALL	CALL	CALL	CALL	CALL	CALL	CALL	CALL	CALL	CALL	CALL	CALL	CALL	CALL	CALL	CALL	CALL
F	CLC	CLC	CLC	CLC	CLC	CLC	CLC	CLC	CLC	CLC	CLC	CLC	CLC	CLC	CLC	CLC	CLC

where

mod	r/m	000	001	010	011	100	101	110	111
Immed		ADD	OR	AOC	SBB	AND	SUB	XOR	CMP
Shift		ROL	ROR	RCL	RCR	SHL/SAL	SHR	SAR	IOIV
Grp 1		TEST	NOT	NEG	MUL	IMUL	DIV	PUSH	
Grp 2		INC	DEC	CALL	CALL	JMP	JMP		

INSTRUCTION SET INDEX

Mnemonic	Page	Mnemonic	Page	Mnemonic	Page
AAA	6	JG	12	MOV	4
AAD	8	JGE	12	MOVS	10
AAM	8	JL	11	MUL	7
AAS	7	JLE	11	NEG	7
ADC	6	JMP	10	NOP	13
ADD	6	JNA	11	NOT	8
AND	9	JNAE	11	OR	9
CALL	10	JNB	12	OUT	5
CBW	8	JNBE	12	POP	4
CLC	13	JNE	12	POPF	5
CLD	14	JNG	11	PUSH	4
CLI	14	JNGE	11	PUSHF	5
CMC	13	JNL	12	RCL	8
CMP	7	JNLE	12	RCR	8
CMPS	10	JNO	12	REP	10
CWD	8	JNP	12	RET	11
DAA	6	JNS	12	ROL	8
DAS	7	JNZ	12	ROR	8
DEC	7	JO	11	SAHF	5
DIV	8	JP	11	SAL	8
ESC	14	JPE	11	SAR	8
HLT	14	JPO	12	SBB	7
IDIV	8	JS	12	SCAS	10
IMUL	7	JZ	11	SHL	8
IN	5	LAHF	5	SHR	8
INC	6	LDS	5	STC	13
INT	13	LEA	5	STD	14
INTO	13	LES	5	STI	14
IRET	13	LOCK	14	STOS	10
JA	12	LODS	10	SUB	6
JAE	12	LOOP	12	TEST	9
JB	11	LOOPE	12	WAIT	14
JBE	11	LOOPNE	12	XCHG	5
JCXZ	12	LOOPNZ	12	XLAT	5
JE	11	LOOPZ	12	XOR	9

Appendix C. Of Characters Keystrokes and Color (U.S. Keyboard Layout

Value	As Characters			As Text Attributes		
				Color/Graphics Monitor Adapter	Monochrome Display Adapter	IBM Display Adapter
Hex	Dec	Symbol	Keystrokes	Background	Foreground	
00	0	Blank (Null)	Ctrl 2	Black	Black	Non-Display
01	1	☺	Ctrl A	Black	Blue	Underline
02	2	☹	Ctrl B	Black	Green	Normal
03	3	♥	Ctrl C	Black	Cyan	Normal
04	4	♦	Ctrl D	Black	Red	Normal
05	5	♣	Ctrl E	Black	Magenta	Normal
06	6	♠	Ctrl F	Black	Brown	Normal
07	7	•	Ctrl G	Black	Light Grey	Normal
08	8	•	Ctrl H, Backspace, Shift Backspace	Black	Dark Grey	Non-Display
09	9	○	Ctrl I	Black	Light Blue	High Intensity Underline
0A	10	○	Ctrl J, Ctrl ↓	Black	Light Green	High Intensity
0B	11	♂	Ctrl K	Black	Light Green	High Intensity
0C	12	♀	Ctrl L	Black	Light Red	High Intensity
0D	13	♪	Ctrl M, ↓, Shift ↓	Black	Light Magenta	High Intensity
0E	14	♫	Ctrl N	Black	Yellow	High Intensity
0F	15	☼	Ctrl O	Black	White	High Intensity
10	16	▲	Ctrl P	Blue	Black	Normal
11	17	▼	Ctrl Q	Blue	Blue	Underline
12	18	↑	Ctrl R	Blue	Green	Normal
13	19	!!	Ctrl S	Blue	Cyan	Normal
14	20	¶	Ctrl T	Blue	Red	Normal
15	21	§	Ctrl U		Magenta	Normal
16	22	■	Ctrl V	Blue	Brown	Normal
17	23	↕	Ctrl W	Blue	Light Grey	Normal

Value		As Text Attributes				
		As Characters			Color/Graphics Monitor Adapter	
Hex	Dec	Symbol	Keystrokes	Modes	Background	Foreground
18	24	!	Ctrl X		Blue	Dark Grey
19	25	,	Ctrl Y		Blue	Light Blue
1A	26	-	Ctrl Z		Blue	Light Green
1B	27	-	Ctrl [, Esc, Shift Esc, Ctrl Esc		Blue	Light Cyan
1C	28	—	Ctrl \		Blue	Light Red
1D	29	↔	Ctrl		Blue	Light Magenta
1E	30	▲	Ctrl 6		Blue	Yellow
1F	31	▼	Ctrl -		Blue	White
20	32	Blank Space	Space Bar, Shift, Space, Ctrl Space, Alt Space		Green	Black
21	33			Shift	Green	Blue
22	34	Shift	Green	Green
23	35	#	#	Shift	Green	Cyan
24	36	\$	\$	Shift	Green	Red
25	37	%	%	Shift	Green	Magenta
26	38	&	&	Shift	Green	Brown
27	39	.	.		Green	Light Grey
28	40	((Shift	Green	Dark Grey
29	41))	Shift	Green	Light Blue
2A	42	*	*	Note 1	Green	Light Green
2B	43	+	+	Shift	Green	Light Cyan
2C	44	,	,		Green	Light Red
2D	45	—	—		Green	Light Magenta
2E	46	.	.	Note 2	Green	Yellow

Value		As Characters			Color/Graphics Monitor Adapter		IBM Monochrome Display Adapter
		Symbol	Keystrokes	Modes	Background	Foreground	
2F	47	/	/		Green	White	High Intensity
30	48	0	0	Note 3	Cyan	Black	Normal
31	49	1	1	Note 3	Cyan	Blue	Underline
32	50	2	2	Note 3	Cyan	Green	Normal
33	51	3	3	Note 3	Cyan	Cyan	Normal
34	52	4	4	Note 3	Cyan	Red	Normal
35	53	5	5	Note 3	Cyan	Magenta	Normal
36	54	6	6	Note 3	Cyan	Brown	Normal
37	55	7	7	Note 3	Cyan	Light Grey	Normal
38	56	8	8	Note 3	Cyan	Dark Grey	High Intensity
39	57	9	9	Note 3	Cyan	Light Blue	High Intensity Underline
3A	58	:	:	Shift	Cyan	Light Green	High Intensity
3B	59	;	;		Cyan	Light Cyan	High Intensity
3C	60	<	<	Shift	Cyan	Light Red	High Intensity
3D	61	=	=		Cyan	Light Magenta	High Intensity
3E	62	>	>	Shift	Cyan	Yellow	High Intensity
3F	63	?	?	Shift	Cyan	White	High Intensity
40	64	@	@	Shift	Red	Black	Normal
41	65	A	A	Note 4	Red	Blue	Underline
42	66	B	B	Note 4	Red	Green	Normal
43	67	C	C	Note 4	Red	Cyan	Normal
44	68	D	D	Note 4	Red	Red	Normal
45	69	E	E	Note 4	Red	Magenta	Normal
46	70	F	F	Note 4	Red	Brown	Normal
47	71	G	G	Note 4	Red	Light Grey	Normal
48	72	H	H	Note 4	Red	Dark Grey	High Intensity
49	73	I	I	Note 4	Red	Light Blue	High Intensity Underline
4A	74	J	J	Note 4	Red	Light Green	High Intensity

Value	As Characters				As Text Attributes		
	Symbol	Keystrokes	Modes	Color/Graphics Monitor Adapter	Background	Foreground	IBM Monochrome Display Adapter
Hex Dec							
4B 75	K	K	Note 4	Red	Red	Light Cyan	High Intensity
4C 76	L	L	Note 4	Red	Red	Light Red	High Intensity
4D 77	M	M	Note 4	Red	Red	Light Magenta	High Intensity
4E 78	N	N	Note 4	Red	Red	Yellow	High Intensity
4F 79	O	O	Note 4	Red	Red	White	High Intensity
50 80	P	P	Note 4	Magenta	Black	Black	Normal
51 81	Q	Q	Note 4	Magenta	Blue	Blue	Underline
52 82	R	R	Note 4	Magenta	Green	Green	Normal
53 83	S	S	Note 4	Magenta	Cyan	Cyan	Normal
54 84	T	T	Note 4	Magenta	Red	Red	Normal
55 85	U	U	Note 4	Magenta	Magenta	Magenta	Normal
56 86	V	V	Note 4	Magenta	Brown	Brown	Normal
57 87	W	W	Note 4	Magenta	Light Grey	Light Grey	Normal
58 88	X	X	Note 4	Magenta	Dark Grey	Dark Grey	High Intensity
59 89	Y	Y	Note 4	Magenta	Light Blue	Light Blue	High Intensity Underline
5A 90	Z	Z	Note 4	Magenta	Light Green	Light Green	High Intensity
5B 91	[[Magenta	Light Cyan	Light Cyan	High Intensity
5C 92	\	\		Magenta	Light Red	Light Red	High Intensity
5D 93]]		Magenta	Light Magenta	Light Magenta	High Intensity
5E 94	^	^	Shift	Magenta	Yellow	Yellow	High Intensity
5F 95	—	—	Shift	Magenta	White	White	High Intensity
60 96	`	`		Yellow	Black	Black	Normal
61 97	a	a	Note 5	Yellow	Blue	Blue	Underline
62 98	b	b	Note 5	Yellow	Green	Green	Normal
63 99	c	c	Note 5	Yellow	Cyan	Cyan	Normal
64 100	d	d	Note 5	Yellow	Red	Red	Normal
65 101	e	e	Note 5	Yellow	Magenta	Magenta	Normal
66 102	f	f	Note 5	Yellow	Brown	Brown	Normal

Value	As Characters				As Text Attributes		
	Symbol	Keystrokes	Modes	Color/Graphics Monitor Adapter	Background	Foreground	IBM Monochrome Display Adapter
Hex Dec							
67 103	g	g	Note 5	Yellow	Light Grey	Light Grey	Normal
68 104	h	h	Note 5	Yellow	Dark Grey	Dark Grey	High Intensity
69 105	i	i	Note 5	Yellow	Light Blue	Light Blue	High Intensity Underline
6A 106	j	j	Note 5	Yellow	Light Green	Light Green	High Intensity
6B 107	k	k	Note 5	Yellow	Light Cyan	Light Cyan	High Intensity
6C 108	l	l	Note 5	Yellow	Light Red	Light Red	High Intensity
6D 109	m	m	Note 5	Yellow	Light Magenta	Light Magenta	High Intensity
6E 110	n	n	Note 5	Yellow	Yellow	Yellow	High Intensity
6F 111	o	o	Note 5	Yellow	White	White	High Intensity
70 112	p	p	Note 5	White	Black	Black	Reverse Video
71 113	q	q	Note 5	White	Blue	Blue	Underline
72 114	r	r	Note 5	White	Green	Green	Normal
73 115	s	s	Note 5	White	Cyan	Cyan	Normal
74 116	f	f	Note 5	White	Red	Red	Normal
75 117	u	u	Note 5	White	Magenta	Magenta	Normal
76 118	v	v	Note 5	White	Brown	Brown	Normal
77 119	w	w	Note 5	White	Light Grey	Light Grey	Normal
78 120	x	x	Note 5	White	Dark Grey	Dark Grey	Reverse Video
79 121	y	y	Note 5	White	Light Blue	Light Blue	High Intensity Underline
7A 122	z	z	Note 5	White	Light Green	Light Green	High Intensity
7B 123	{	{	Shift	White	Light Cyan	Light Cyan	High Intensity
7C 124			Shift	White	Light Red	Light Red	High Intensity
7D 125	}	}	Shift	White	Light Magenta	Light Magenta	High Intensity
7E 126	~	~	Shift	White	Yellow	Yellow	High Intensity
7F 127	Δ	Ctrl —		White	White	White	High Intensity

Value	As Text Attributes			
	As Characters		Color/Graphics Monitor Adapter	
Hex/Dec	Symbol	Keystrokes	Background	Foreground
80 to FF Hex are Flashing in both Color & IBM Monochrome * * * *				
80 128	Ç	Alt 128	Black	Black
81 129	ü	Alt 129	Black	Blue
82 130	é	Alt 130	Black	Green
83 131	â	Alt 131	Black	Cyan
84 132	ä	Alt 132	Black	Red
85 133	à	Alt 133	Black	Magenta
86 134	ã	Alt 134	Black	Brown
87 135	ç	Alt 135	Black	Light Grey
88 136	ê	Alt 136	Black	Dark Grey
89 137	ë	Alt 137	Black	Light Blue
8A 138	è	Alt 138	Black	Light Green
8B 139	ì	Alt 139	Black	Light Cyan
8C 140	î	Alt 140	Black	Light Red
8D 141	ï	Alt 141	Black	Light Magenta
8E 142	À	Alt 142	Black	Yellow
8F 143	Á	Alt 143	Black	White
90 144	É	Alt 144	Blue	Black
91 145	æ	Alt 145	Blue	Blue
92 146	Æ	Alt 146	Blue	Green
93 147	ô	Alt 147	Blue	Cyan
94 148	ö	Alt 148	Blue	Red
95 149	ò	Alt 149	Blue	Magenta
96 150	û	Alt 150	Blue	Brown
97 151	ü	Alt 151	Blue	Light Grey
98 152	ÿ	Alt 152	Blue	Dark Grey
99 153	ö	Alt 153	Blue	Light Blue
9A 154	ü	Alt 154	Blue	Light Green

Value	As Characters				As Text Attributes		
	Hex/Dec	Symbol	Keystrokes	Modes	Background	Color/Graphics Monitor Adapter	IBM Monochrome Display Adapter
9B 155	c	Alt 155	Note 6	Note 6	Blue	Light Cyan	High Intensity
9C 156	£	Alt 156	Note 6	Note 6	Blue	Light Red	High Intensity
9D 157	¥	Alt 157	Note 6	Note 6	Blue	Light Magenta	High Intensity
9E 158	Pt	Alt 158	Note 6	Note 6	Blue	Yellow	High Intensity
9F 159	/	Alt 159	Note 6	Note 6	Blue	White	High Intensity
A0 160	ä	Alt 160	Note 6	Note 6	Green	Black	Normal
A1 161	ï	Alt 161	Note 6	Note 6	Green	Blue	Underline
A2 162	ó	Alt 162	Note 6	Note 6	Green	Green	Normal
A3 163	ú	Alt 163	Note 6	Note 6	Green	Cyan	Normal
A4 164	ñ	Alt 164	Note 6	Note 6	Green	Red	Normal
A5 165	Ñ	Alt 165	Note 6	Note 6	Green	Magenta	Normal
A6 166	ä	Alt 166	Note 6	Note 6	Green	Brown	Normal
A7 167	ö	Alt 167	Note 6	Note 6	Green	Light Grey	Normal
A8 168	¿	Alt 168	Note 6	Note 6	Green	Dark Grey	High Intensity
A9 169	—	Alt 169	Note 6	Note 6	Green	Light Blue	High Intensity Underline
AA 170	—	Alt 170	Note 6	Note 6	Green	Light Green	High Intensity
AB 171	½	Alt 171	Note 6	Note 6	Green	Light Cyan	High Intensity
AC 172	¼	Alt 172	Note 6	Note 6	Green	Light Red	High Intensity
AD 173	ı	Alt 173	Note 6	Note 6	Green	Light Magenta	High Intensity
AE 174	<<	Alt 174	Note 6	Note 6	Green	Yellow	High Intensity
AF 175	>>	Alt 175	Note 6	Note 6	Green	White	High Intensity
B0 176	⋮	Alt 176	Note 6	Note 6	Cyan	Black	Normal
B1 177	⋮	Alt 177	Note 6	Note 6	Cyan	Blue	Underline
B2 178	⋮	Alt 178	Note 6	Note 6	Cyan	Green	Normal
B3 179	⋮	Alt 179	Note 6	Note 6	Cyan	Cyan	Normal
B4 180	⋮	Alt 180	Note 6	Note 6	Cyan	Red	Normal
B5 181	⋮	Alt 181	Note 6	Note 6	Cyan	Magenta	Normal
B6 182	⋮	Alt 182	Note 6	Note 6	Cyan	Brown	Normal

Value		As Characters				As Text Attributes		
		Color/Graphics Monitor Adapter		IBM Monochrome Display Adapter				
Hex	Dec	Symbol	Keystrokes	Modes	Background	Foreground		
B7	183		Alt 183	Note 6	Cyan	Light Grey	Normal	
B8	184		Alt 184	Note 6	Cyan	Dark Grey	High Intensity	
B9	185		Alt 185	Note 6	Cyan	Light Blue	High Intensity Underline	
BA	186		Alt 186	Note 6	Cyan	Light Green	High Intensity	
BB	187		Alt 187	Note 6	Cyan	Light Cyan	High Intensity	
BC	188		Alt 188	Note 6	Cyan	Light Red	High Intensity	
BD	189		Alt 189	Note 6	Cyan	Light Magenta	High Intensity	
BE	190		Alt 190	Note 6	Cyan	Yellow	High Intensity	
BF	191		Alt 191	Note 6	Cyan	White	High Intensity	
C0	192		Alt 192	Note 6	Red	Black	Normal	
C1	193		Alt 193	Note 6	Red	Blue	Underline	
C2	194		Alt 194	Note 6	Red	Green	Normal	
C3	195		Alt 195	Note 6	Red	Cyan	Normal	
C4	196		Alt 196	Note 6	Red	Red	Normal	
C5	197		Alt 197	Note 6	Red	Magenta	Normal	
C6	198		Alt 198	Note 6	Red	Brown	Normal	
C7	199		Alt 199	Note 6	Red	Light Grey	Normal	
C8	200		Alt 200	Note 6	Red	Dark Grey	High Intensity	
C9	201		Alt 201	Note 6	Red	Light Blue	High Intensity Underline	
CA	202		Alt 202	Note 6	Red	Light Green	High Intensity	
CB	203		Alt 203	Note 6	Red	Light Cyan	High Intensity	
CC	204		Alt 204	Note 6	Red	Light Red	High Intensity	
CD	205		Alt 205	Note 6	Red	Light Magenta	High Intensity	
CE	206		Alt 206	Note 6	Red	Yellow	High Intensity	
CF	207		Alt 207	Note 6	Red	White	High Intensity	
D0	208		Alt 208	Note 6	Magenta	Black	Normal	

Value	As Characters				As Text Attributes		
	Hex	Dec	Symbol	Keystrokes	Modes	Color/Graphics Monitor Adapter	IBM Monochrome Display Adapter
D1	209		Alt 209	Note 6	Magenta	Blue	Underline
D2	210		Alt 210	Note 6	Magenta	Green	Normal
D3	211		Alt 211	Note 6	Magenta	Cyan	Normal
D4	212		Alt 212	Note 6	Magenta	Red	Normal
D5	213		Alt 213	Note 6	Magenta	Magenta	Normal
D6	214		Alt 214	Note 6	Magenta	Brown	Normal
D7	215		Alt 215	Note 6	Magenta	Light Grey	Normal
D8	216		Alt 216	Note 6	Magenta	Dark Grey	High Intensity
D9	217		Alt 217	Note 6	Magenta	Light Blue	High Intensity Underline
DA	218		Alt 218	Note 6	Magenta	Light Green	High Intensity
DB	219		Alt 219	Note 6	Magenta	Light Cyan	High Intensity
DC	220		Alt 220	Note 6	Magenta	Light Red	High Intensity
DD	221		Alt 221	Note 6	Magenta	Light Magenta	High Intensity
DE	222		Alt 222	Note 6	Magenta	Yellow	High Intensity
DF	223		Alt 223	Note 6	Magenta	White	High Intensity
E0	224		Alt 224	Note 6	Yellow	Black	Normal
E1	225		Alt 225	Note 6	Yellow	Blue	Underline
E2	226		Alt 226	Note 6	Yellow	Green	Normal
E3	227		Alt 227	Note 6	Yellow	Cyan	Normal
E4	228		Alt 228	Note 6	Yellow	Red	Normal
E5	229		Alt 229	Note 6	Yellow	Magenta	Normal
E6	230		Alt 230	Note 6	Yellow	Brown	Normal
E7	231		Alt 231	Note 6	Yellow	Light Grey	Normal
E8	232		Alt 232	Note 6	Yellow	Dark Grey	High Intensity
E9	233		Alt 233	Note 6	Yellow	Light Blue	High Intensity Underline
EA	234		Alt 234	Note 6	Yellow	Light Green	High Intensity
EB	235		Alt 235	Note 6	Yellow	Light Cyan	High Intensity

Value	As Characters			As Text Attributes		
	Symbol	Keystrokes	Modes	Color/Graphics Monitor Adapter	Background	IBM Monochrome Display Adapter
Hex Dec						
EC 236	∞	Alt 236	Note 6	Yellow	Light Red	High Intensity
ED 237	φ	Alt 237	Note 6	Yellow	Light Magenta	High Intensity
EE 238	€	Alt 238	Note 6	Yellow	Yellow	High Intensity
EF 239	∩	Alt 239	Note 6	Yellow	White	High Intensity
FO 240	≡	Alt 240	Note 6	White	Black	Reverse Video
F1 241	±	Alt 241	Note 6	White	Blue	Underline
F2 242	≈	Alt 242	Note 6	White	Green	Normal
F3 243	∇	Alt 243	Note 6	White	Cyan	Normal
F4 244	∩	Alt 244	Note 6	White	Red	Normal
F5 245	∩	Alt 245	Note 6	White	Magenta	Normal
F6 246	÷	Alt 246	Note 6	White	Brown	Normal
F7 247	≈	Alt 247	Note 6	White	Light Grey	Normal
F8 248	○	Alt 248	Note 6	White	Dark Grey	Reverse Video
F9 249	●	Alt 249	Note 6	White	Light Blue	High Intensity Underline
FA 250	•	Alt 250	Note 6	White	Light Green	High Intensity
FB 251	√	Alt 251	Note 6	White	Light Cyan	High Intensity
FC 252	η	Alt 252	Note 6	White	Light Red	High Intensity
FD 253	2	Alt 253	Note 6	White	Light Magenta	High Intensity
FE 254	■	Alt 254	Note 6	White	Yellow	High Intensity
FF 255	BLANK	Alt 255	Note 6	White	White	High Intensity

NOTE 1 Asterisk (*) can easily be keyed using two methods:
1) hit the **Prt Sc** key or 2) in shift mode hit the ***** key.

NOTE 2 Period (.) can easily be keyed using two methods:
1) hit the **.** key or 2) in shift or Num Lock mode hit the **Del** key.

NOTE 3 Numeric characters (0—9) can easily be keyed using two methods: 1) hit the numeric keys on the top row of the typewriter portion of the keyboard or 2) in shift or Num Lock mode hit the numeric keys in the 10—key pad portion of the keyboard.

NOTE 4 Upper case alphabetic characters (A—Z) can easily be keyed in two modes: 1) in shift mode the appropriate alphabetic key or 2) in Caps Lock mode hit the appropriate alphabetic key.

NOTE 5 Lower case alphabetic characters (a—z) can easily be keyed in two modes: 1) in "normal" mode hit the appropriate key or 2) in Caps Lock combined with shift mode hit the appropriate alphabetic key.

NOTE 6 The 3 digits after the Alt key must be typed from the numeric key pad (keys 71—73, 75—77, 79—82). Character codes 000 through 255 can be entered in this fashion. (With Caps Lock activated, Character codes 97 through 122 will display upper case rather than lower case alphabetic characters.)

Character Set (00-7F) Quick Reference

DECIMAL VALUE	HEXA DECIMAL VALUE	0	16	32	48	64	80	96	112
HEXA DECIMAL VALUE	DECIMAL VALUE	0	1	2	3	4	5	6	7
0	0	BLANK (NULL)	►	BLANK (SPACE)	0	@	P	,	p
1	1	☺	◄	!	1	A	Q	a	q
2	2	☹	↕	"	2	B	R	b	r
3	3	♥	!!	#	3	C	S	c	s
4	4	♦	¶	\$	4	D	T	d	t
5	5	♣	§	%	5	E	U	e	u
6	6	♠	■	&	6	F	V	f	v
7	7	•	↑↓	'	7	G	W	w	w
8	8	•	↑	(8	H	X	h	x
9	9	○	↓)	9	I	Y	i	y
10	A	◯	→	*	:	J	Z	j	z
11	B	♂	←	+	;	K	I	k	{
12	C	♀	└	,	<	L	/	l	!
13	D	♪	↔	—	=	M	I	m	}
14	E	♪	◄	.	>	N	^	n	~
15	F	☼	►	/	?	O	_	o	Δ

Character Set (80-FF) Quick Reference

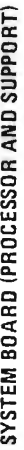
DECIMAL VALUE	HEXA DECIMAL VALUE	128	144	160	176	192	208	224	240
HEXA DECIMAL VALUE	DECIMAL VALUE	8	9	A	B	C	D	E	F
0	0	Ç	É	á	▤	▤	▤	∞	≡
1	1	ü	æ	í	▥	▥	▥	β	±
2	2	é	Æ	ó	▦	▦	▦	Γ	△
3	3	â	ô	ú	▧	▧	▧	π	∇
4	4	ä	ö	ñ	▨	▨	▨	Σ	∫
5	5	á	ò	Ñ	▩	▩	▩	σ	÷
6	6	ã	û	ä	▪	▪	▪	ρ	≈
7	7	ç	ù	ó	▫	▫	▫	τ	◦
8	8	ê	ÿ	¿	▬	▬	▬	ø	•
9	9	ë	Ö	┐	▮	▮	▮	θ	•
10	A	è	Ü	┐	▯	▯	▯	Ω	•
11	B	ï	ç	½	▰	▰	▰	δ	√
12	C	î	£	¼	▱	▱	▱	∞	n
13	D	ï	¥	ì	▲	▲	▲	φ	2
14	E	Ä	℞	«	△	△	△	∈	■
15	F	Å	ƒ	»	▴	▴	▴	∪	BLANK 'FF'

APPENDIX D. LOGIC DIAGRAMS

Contents

System Board	D-2
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IBM Monochrome Display And Parallel Printer Adapter	D-14
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IBM 80 CPS Graphics Printer	D-33
Parallel Printer Adapter	D-36
5 1/4" Diskette Drive Adapter	D-37
5 1/4" Diskette Drive	D-41
32KB Memory Expansion Option	D-44
64KB Memory Expansion Option	D-47
64/256KB Memory Expansion Option	D-50
Asynchronous Communications Adapter	D-54
Game Control Adapter	D-55
Prototype Card	D-56

SYSTEM BOARD (WAIT STATE GENERATOR)

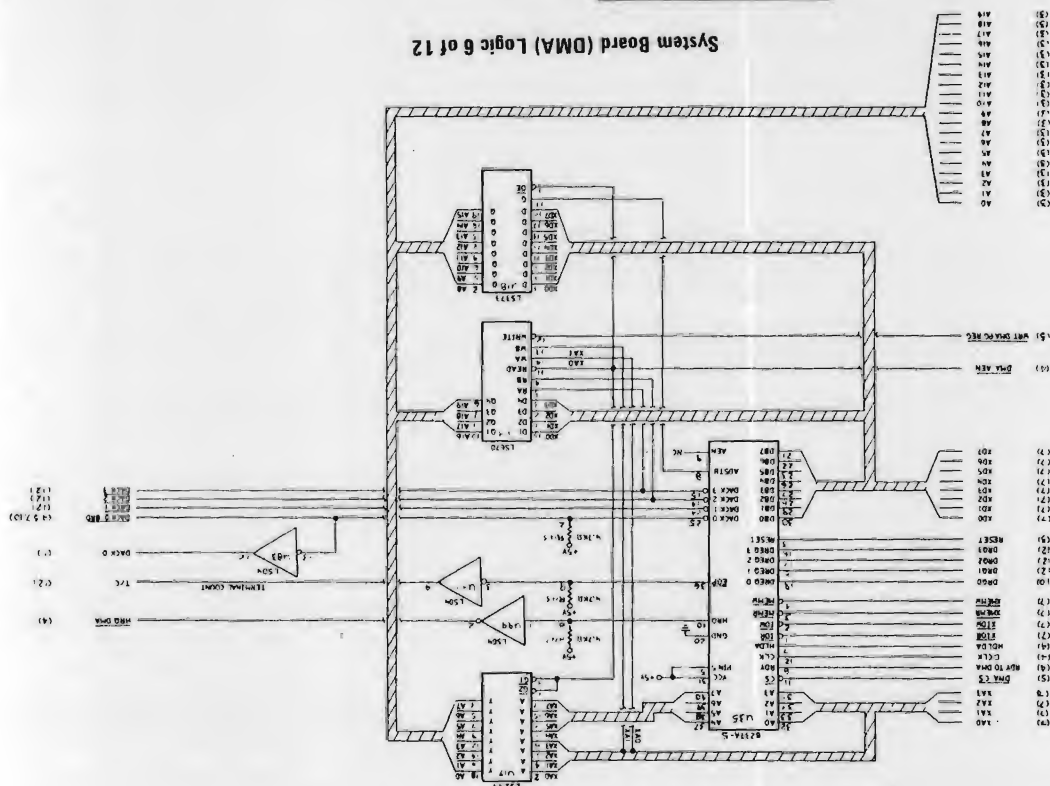


Note: Logics one and two of twelve are not applicable

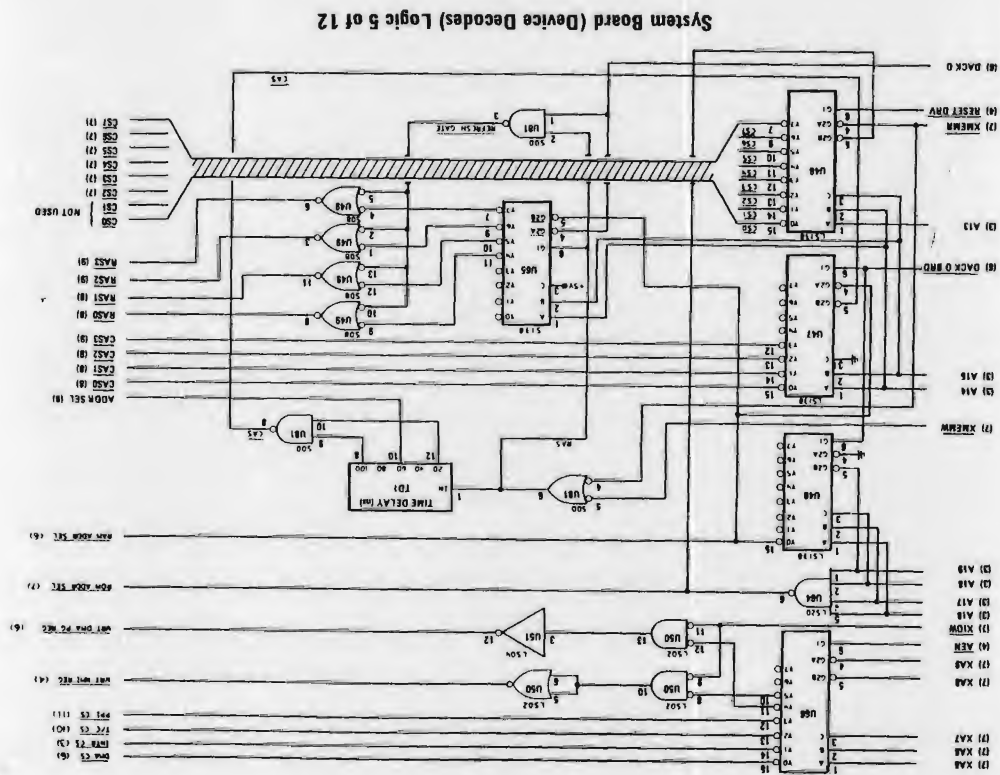


Note: Logics one and two of twelve are not applicable

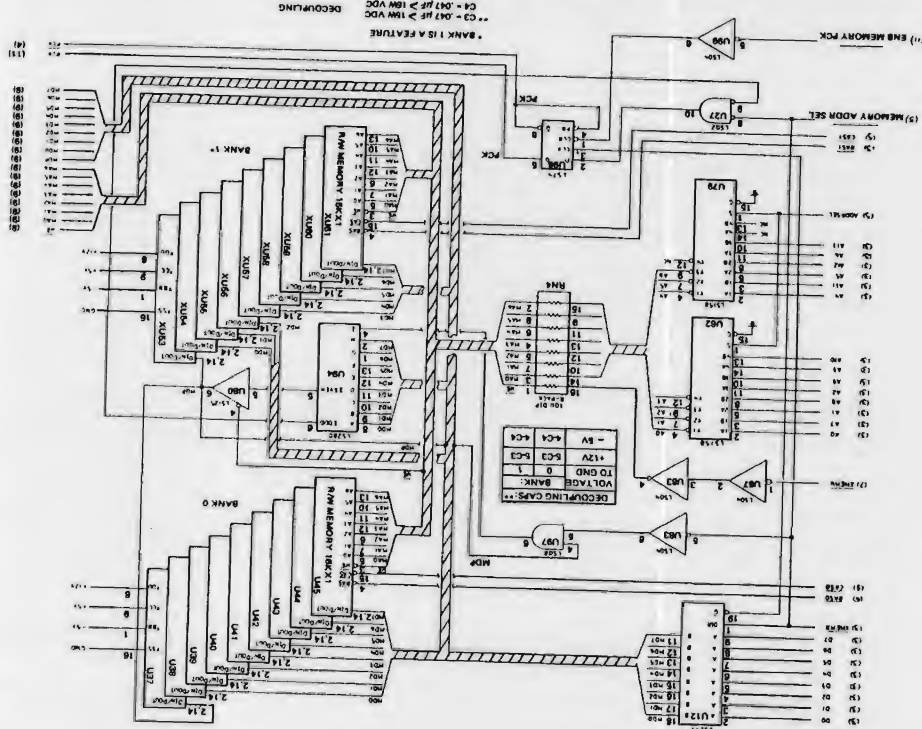
SYSTEM BOARD (DMA)



SYSTEM BOARD (DEVICE DECODES)

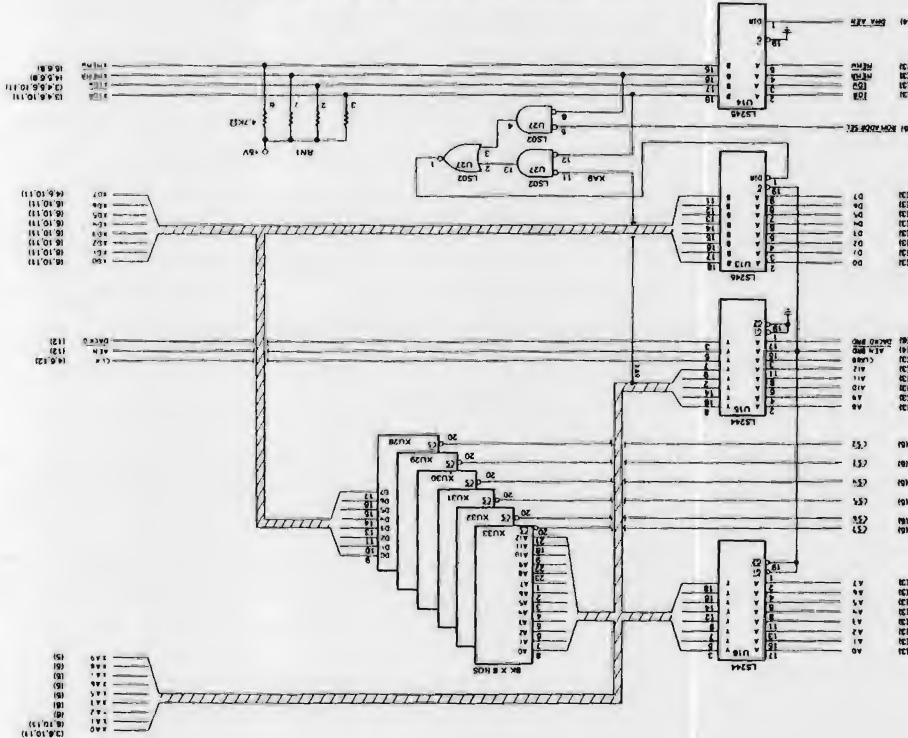


System Board (Dynamic Memory) Logic 8 of 12



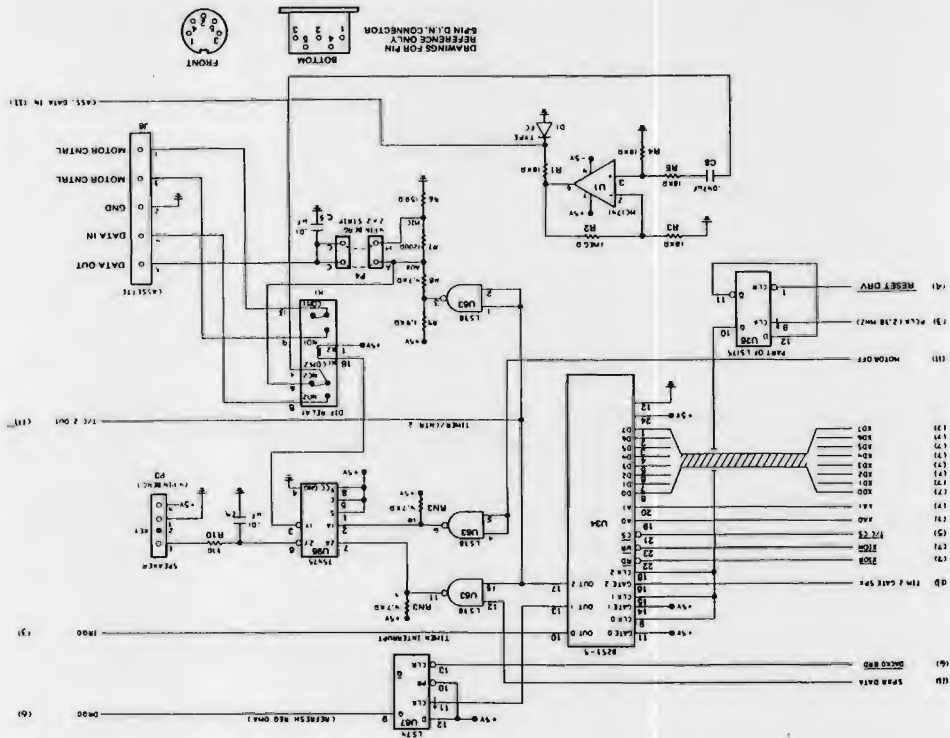
SYSTEM BOARD (DYNAMIC MEMORY)

System Board (ROS And Bus Driver) Logic 7 of 12

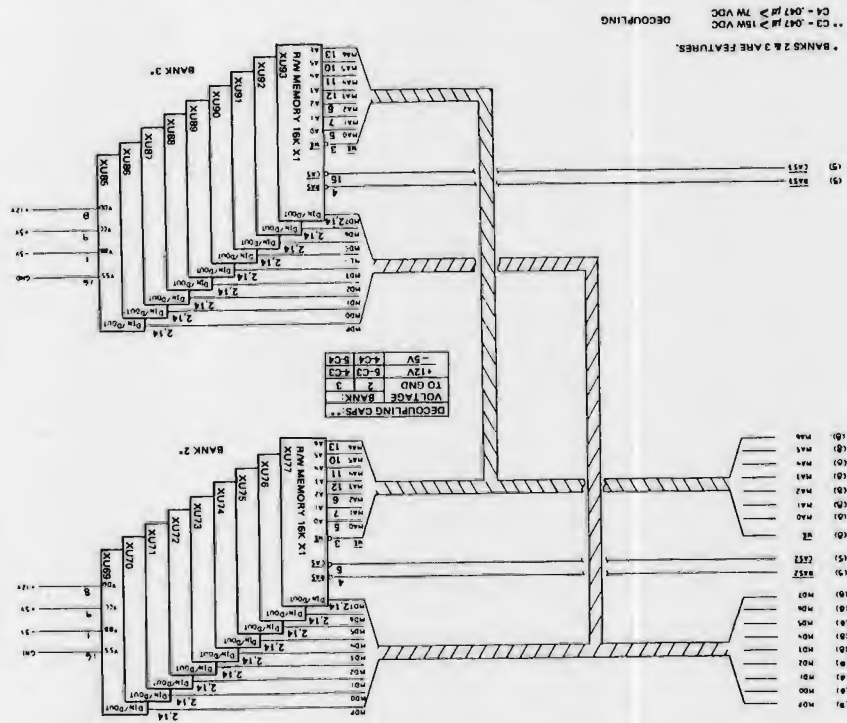


SYSTEM BOARD (ROS AND BUS DRIVER)

SYSTEM BOARD (SPEAKER/CASSETTE/TIMER/COUNTER)

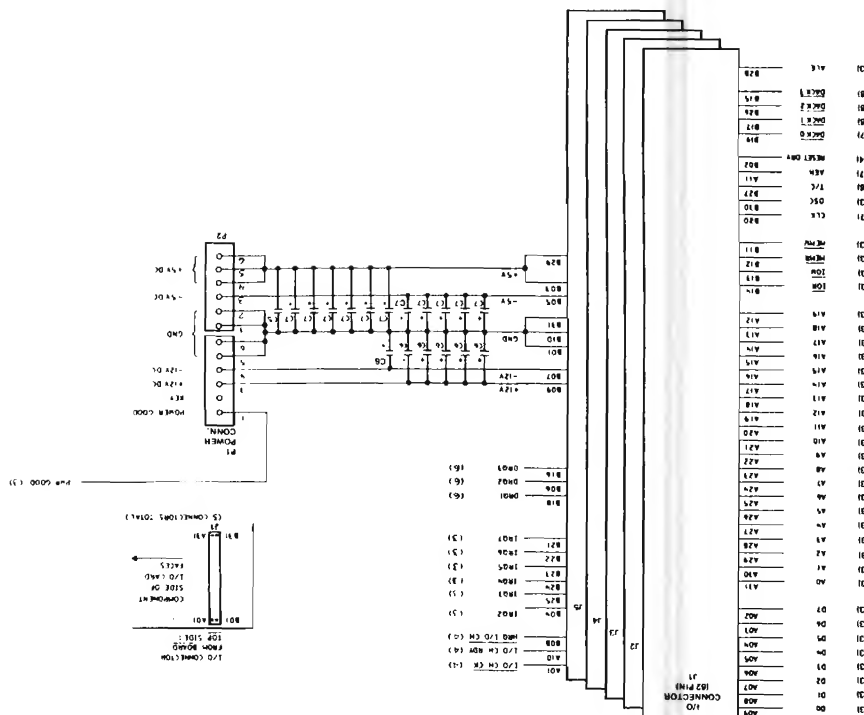


SYSTEM BOARD (DYNAMIC MEMORY EXTENDED)



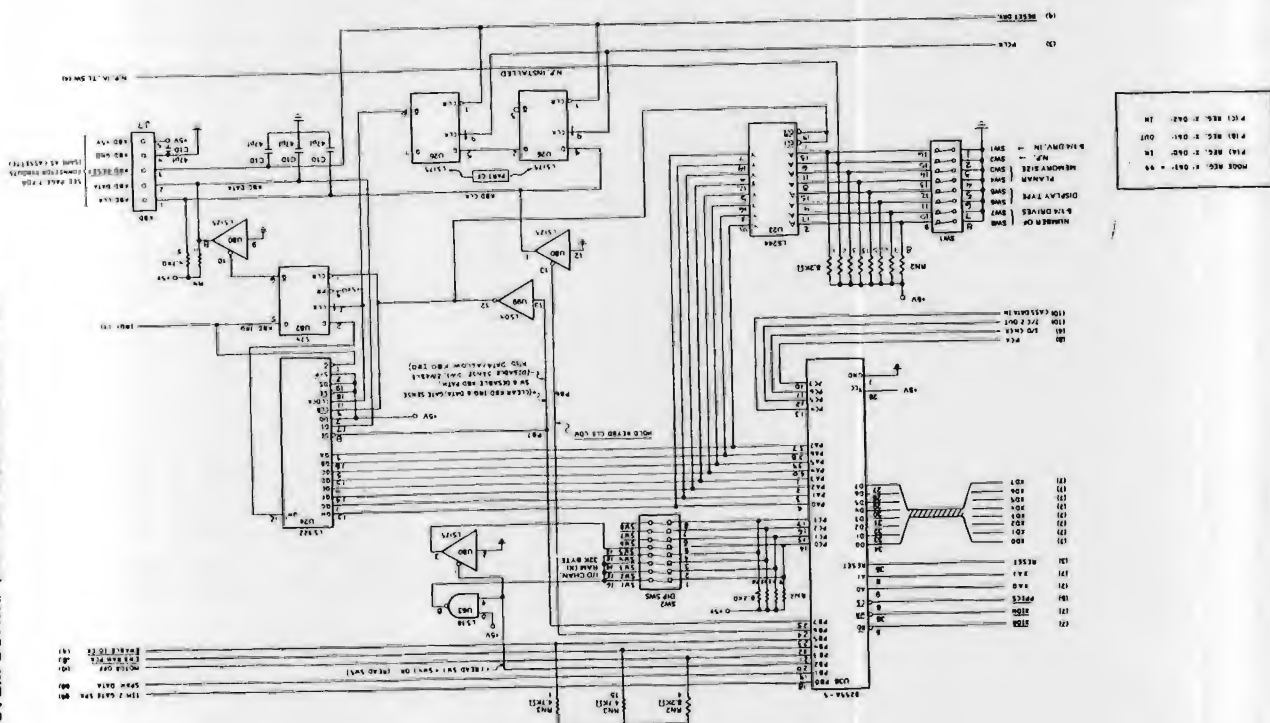
System Board (I/O Channel) Logic 12 of 12

NOTE: ALL CAPS ARE 8255 TRANSISTOR ON THIS PAGE



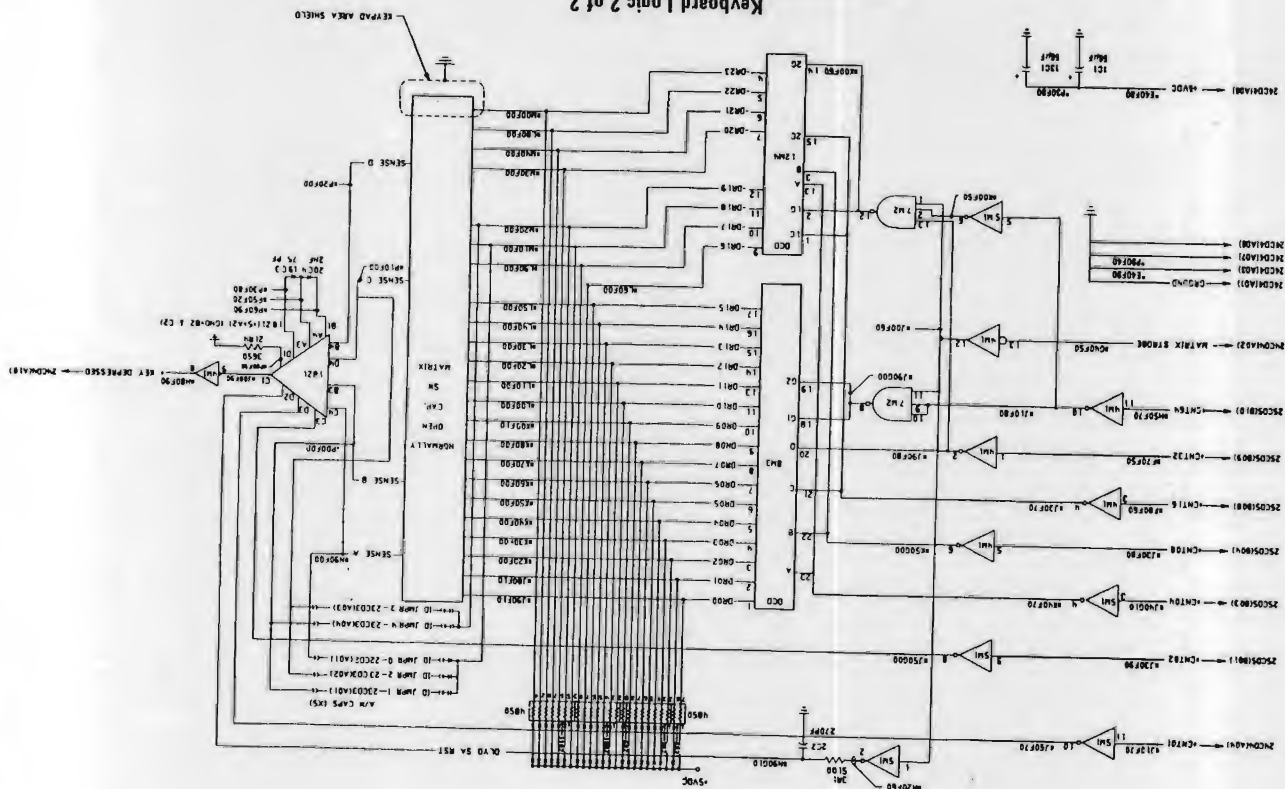
SYSTEM BOARD (I/O CHANNEL)

System Board (Keyboard/Sense/Control) Logic 11 of 12

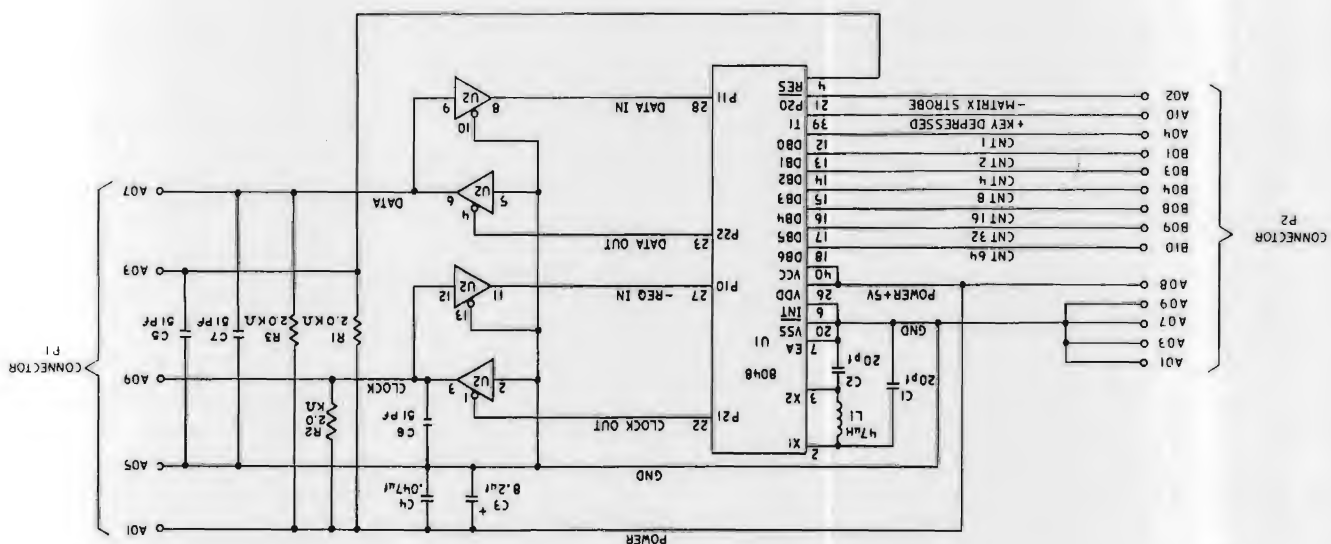


SYSTEM BOARD (KEYBOARD/SENSE/CONTROL)

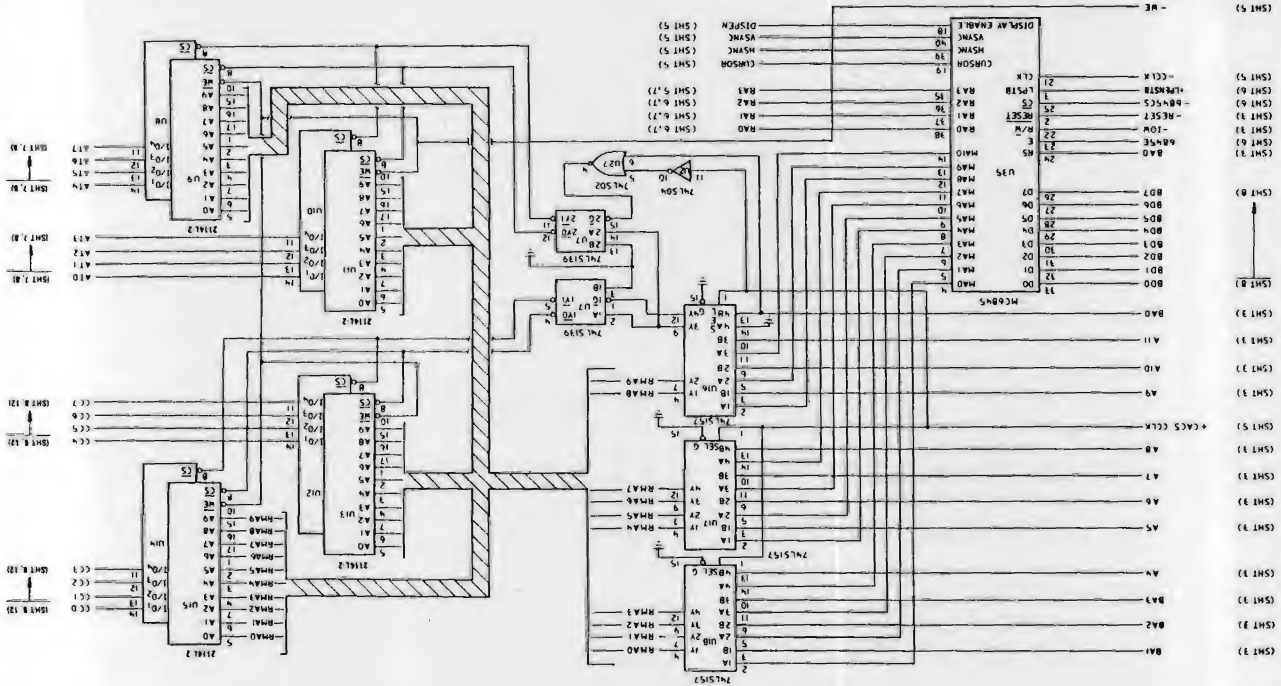
Keyboard Logic 2 of 2



Keyboard Logic 1 of 2

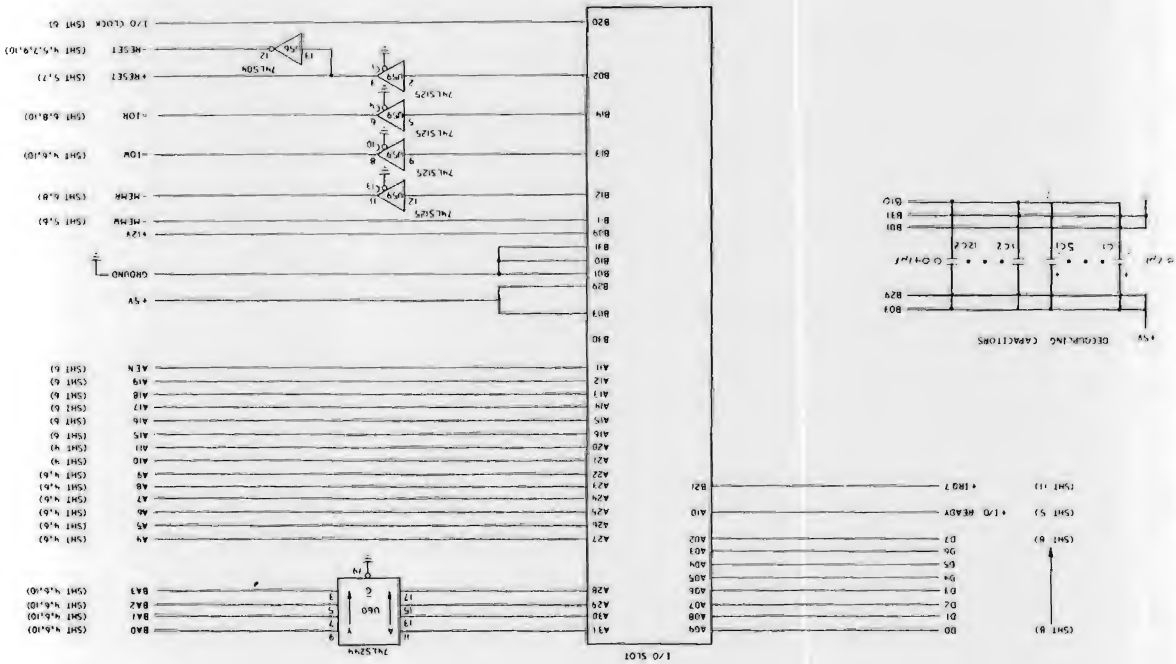


IBM MONOCHROME DISPLAY AND PARALLEL PRINTER ADAPTER

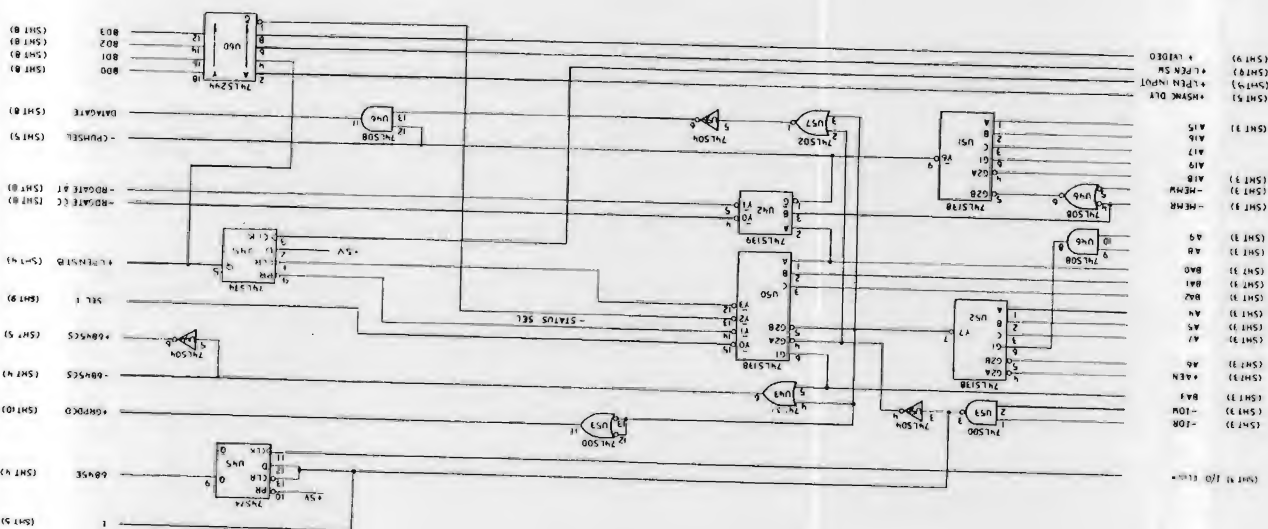


IBM Monochrome Display And Parallel Printer Adapter Logic 3 of 12

IBM MONOCHROME DISPLAY AND PARALLEL PRINTER ADAPTER

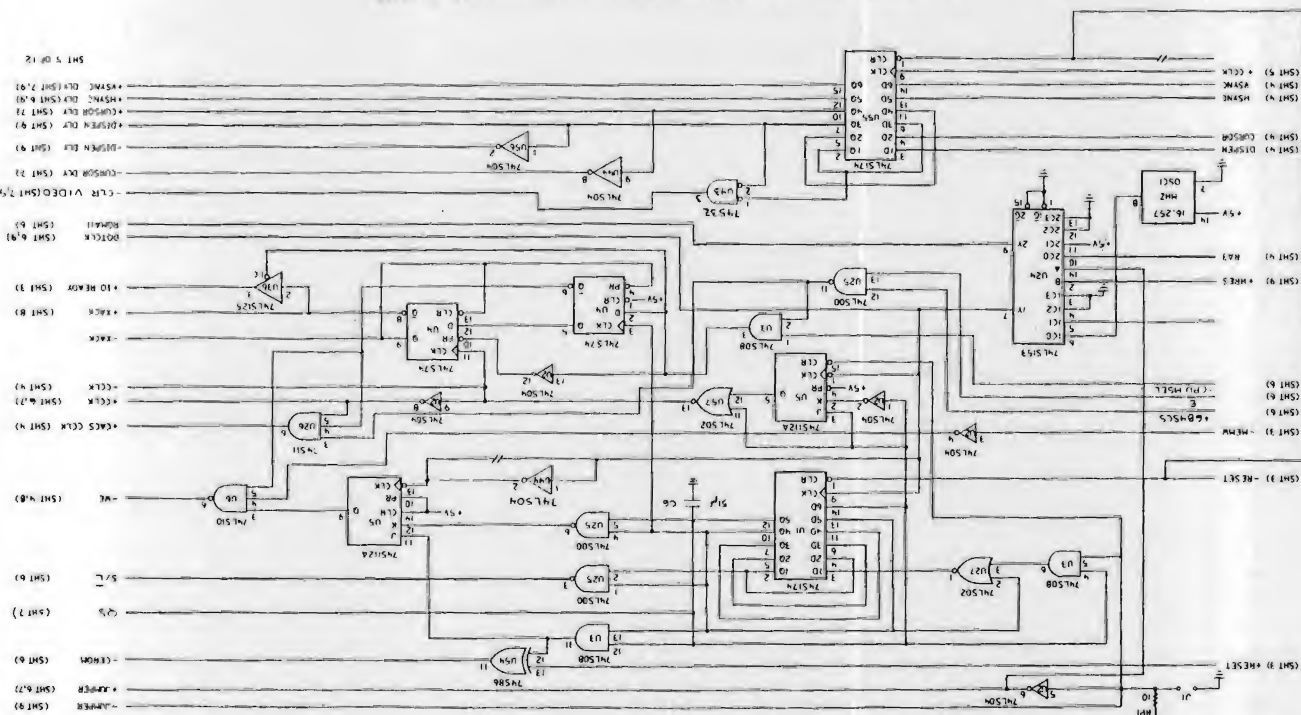


IBM MONOCHROME DISPLAY AND PARALLEL PRINTER ADAPTER



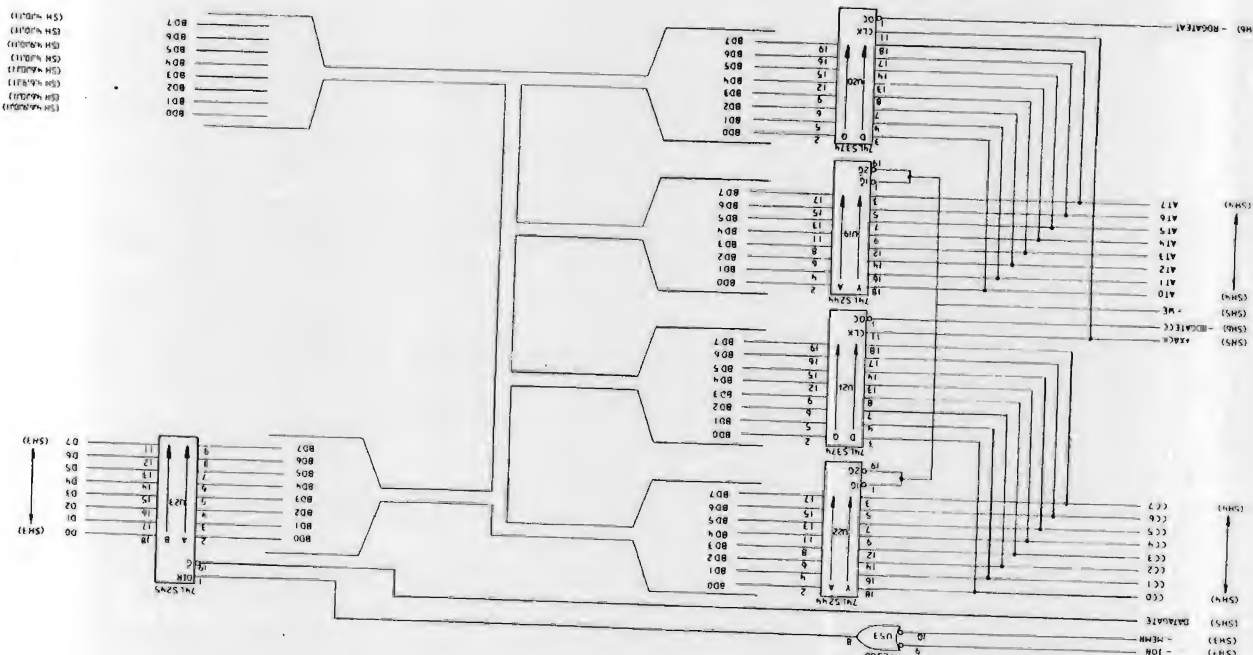
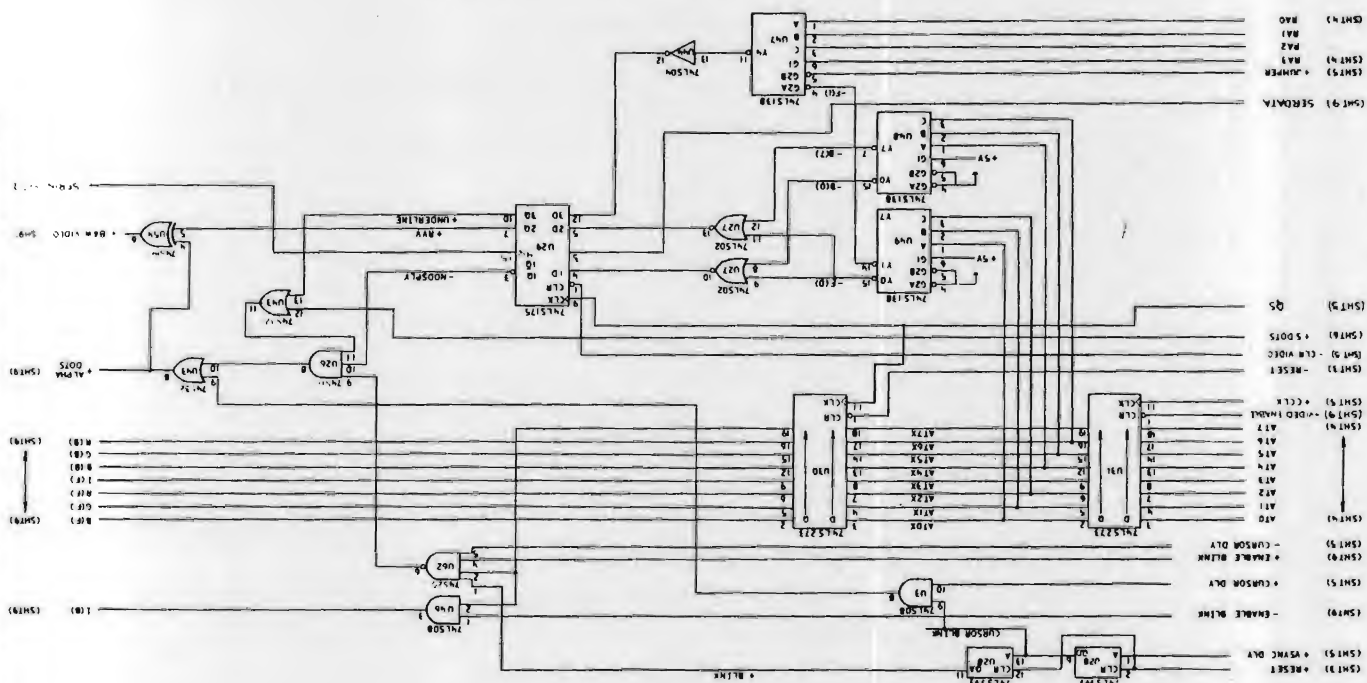
IBM Monochrome Display And Parallel Printer Adapter Logic 5 of 12

IBM MONOCHROME DISPLAY AND PARALLEL PRINTER ADAPTER

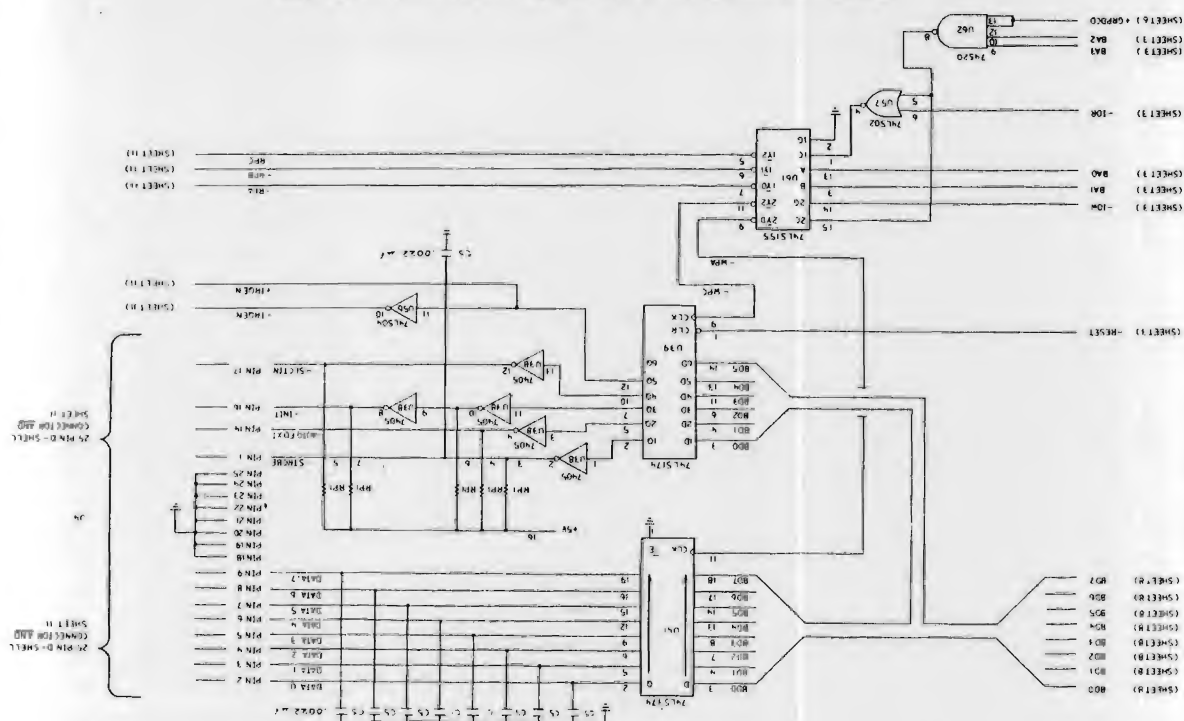


D-18

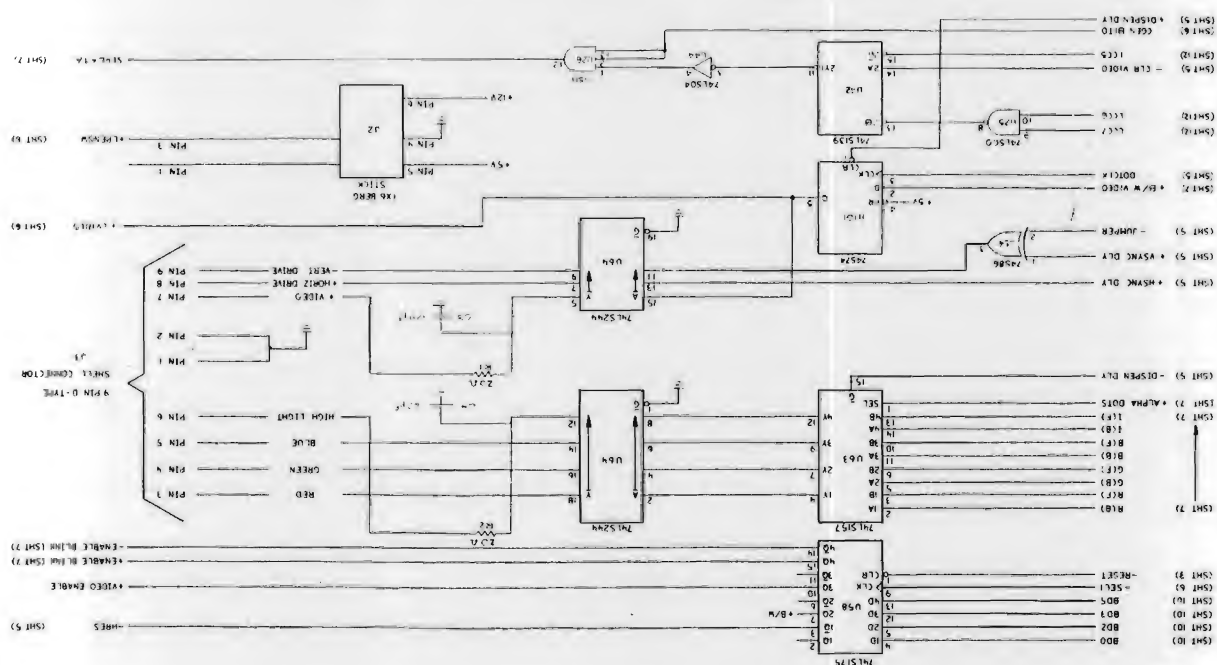
BM MONOCHROME DISPLAY AND PARALLEL PRINTER ADAPTER



IBM Monochrome Display And Parallel Printer Adapter Logic 10 of 12



IBM Monochrome Display And Parallel Printer Adapter Logic 9 of 12

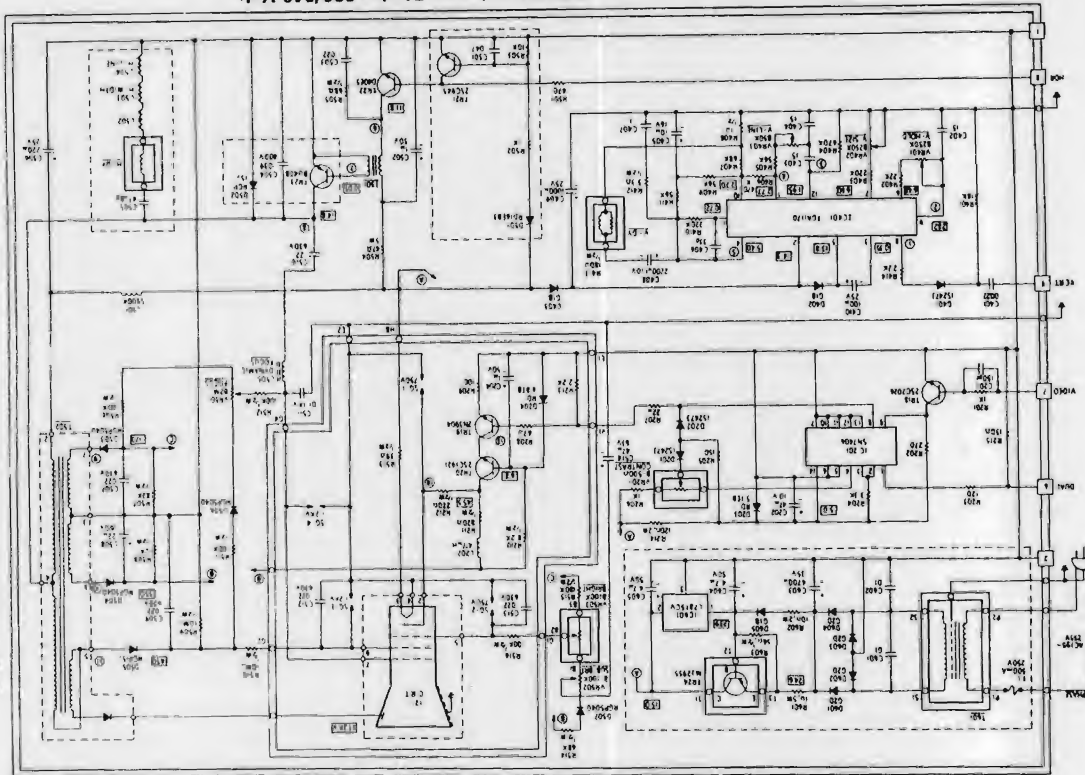


IBM Monochrome Display 220/240 Volt

NOTES:
1. SYSTEM VOLTAGES ARE IN CONFORMITY WITH IEC 60060-1:1980.
2. ALL VOLTAGES ARE RMS EXCEPT WHERE SHOWN OTHERWISE.
3. ALL CAPACITORS ARE NEW EXCEPT WHERE SHOWN OTHERWISE.
4. CAPACITORS ARE NEW EXCEPT WHERE SHOWN OTHERWISE.
5. CAPACITORS ARE NEW EXCEPT WHERE SHOWN OTHERWISE.
6. CAPACITORS ARE NEW EXCEPT WHERE SHOWN OTHERWISE.
7. CAPACITORS ARE NEW EXCEPT WHERE SHOWN OTHERWISE.
8. CAPACITORS ARE NEW EXCEPT WHERE SHOWN OTHERWISE.
9. CAPACITORS ARE NEW EXCEPT WHERE SHOWN OTHERWISE.
10. CAPACITORS ARE NEW EXCEPT WHERE SHOWN OTHERWISE.

IBM Monochrome Display

DANGER
HAZARDOUS VOLTAGES UP TO 450 VOLTS EXIST ON THE PRINTED CIRCUIT BOARDS

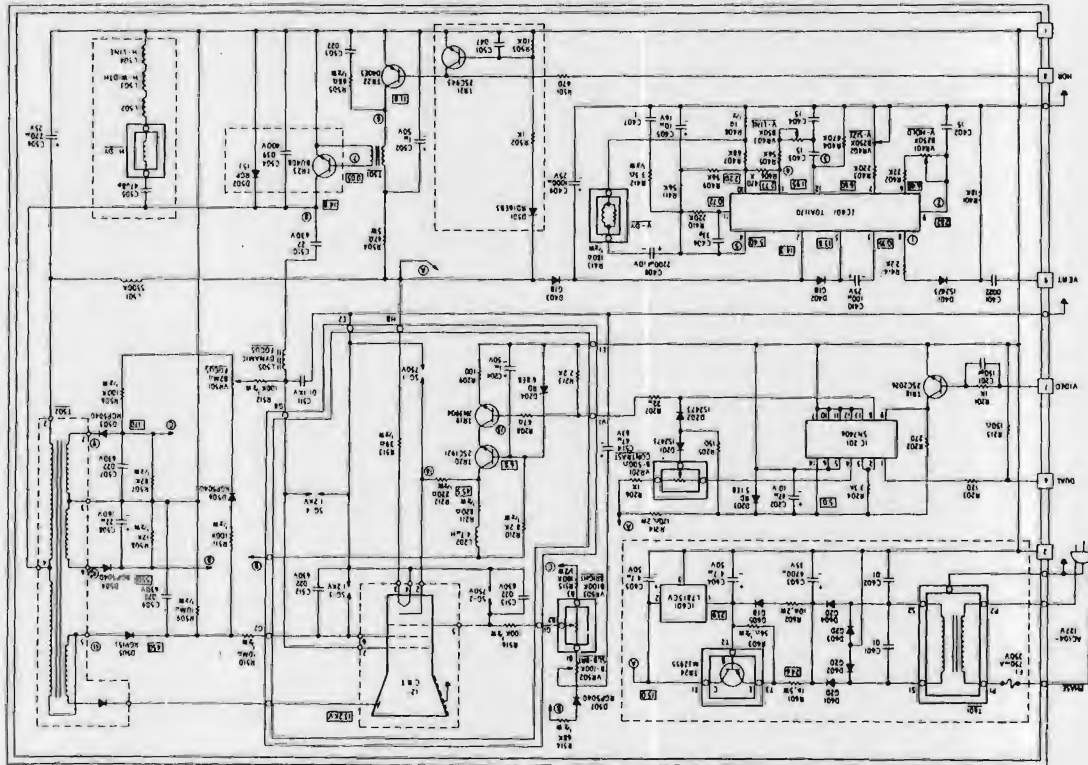


IBM Monochrome Display 120 Volt

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4. CAPACITORS ARE NEW EXCEPT WHERE SHOWN OTHERWISE.
5. CAPACITORS ARE NEW EXCEPT WHERE SHOWN OTHERWISE.
6. CAPACITORS ARE NEW EXCEPT WHERE SHOWN OTHERWISE.
7. CAPACITORS ARE NEW EXCEPT WHERE SHOWN OTHERWISE.
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10. CAPACITORS ARE NEW EXCEPT WHERE SHOWN OTHERWISE.

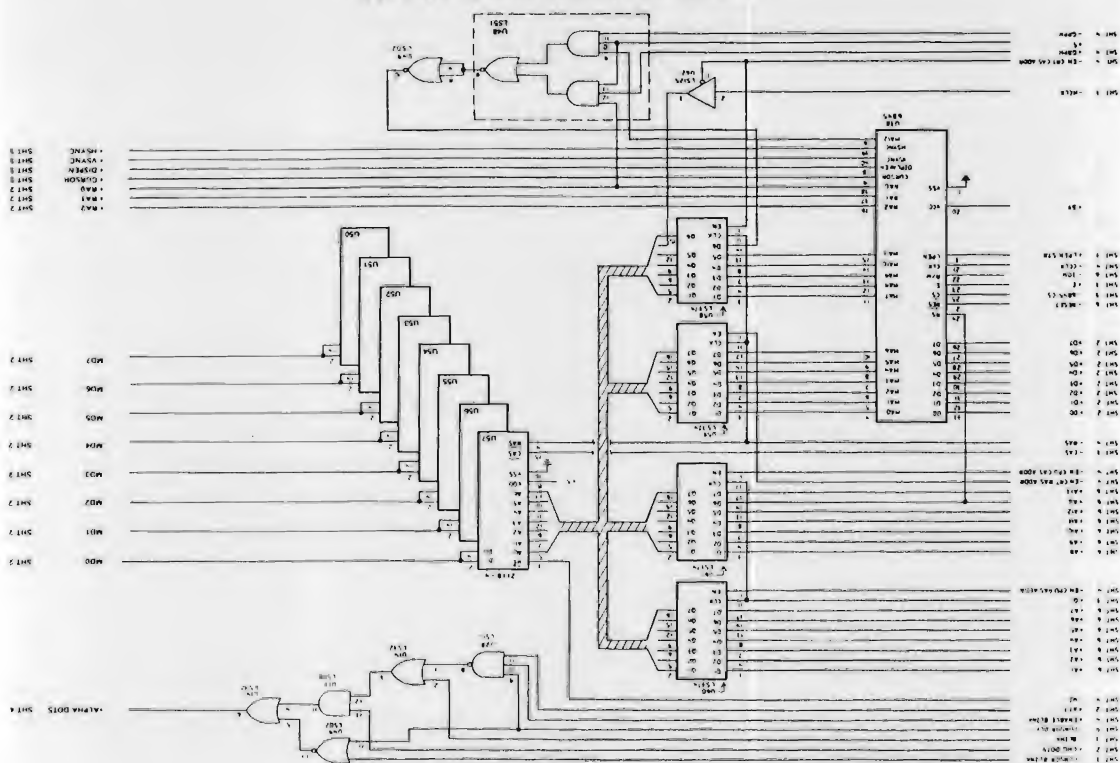
IBM MONOCHROME DISPLAY

DANGER
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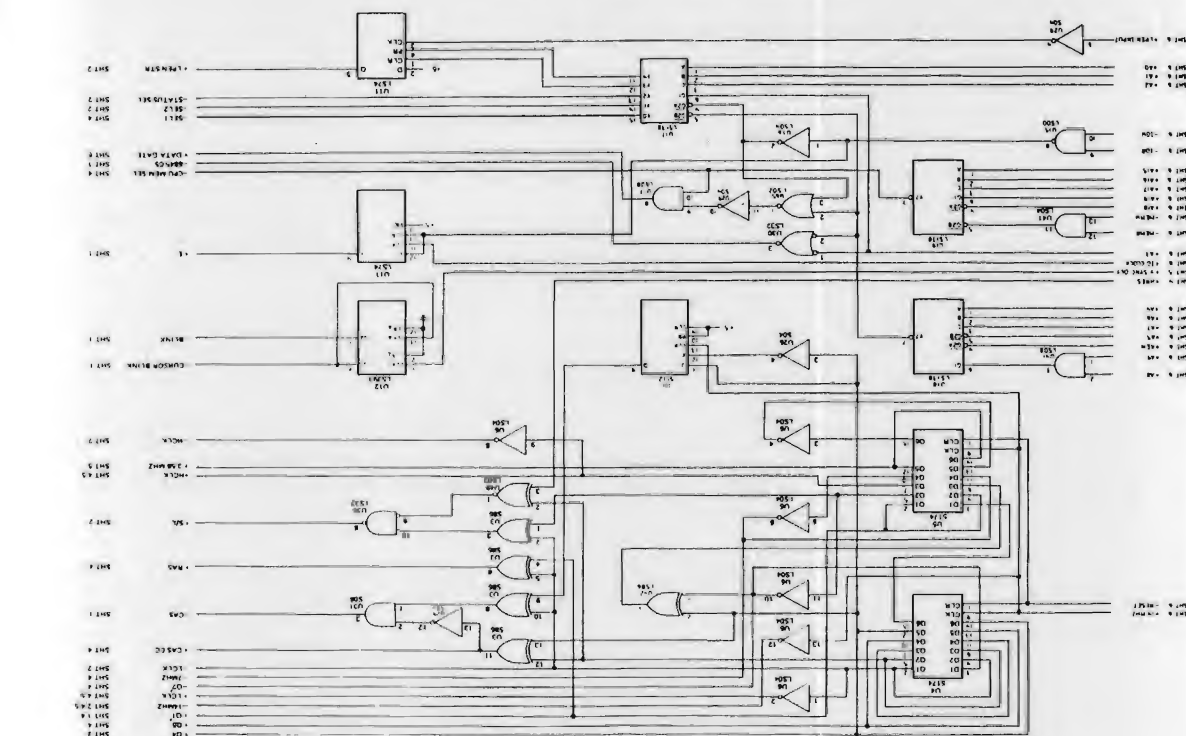
COLOR/GRAPHICS MONITOR ADAPTER

APPENDIX D



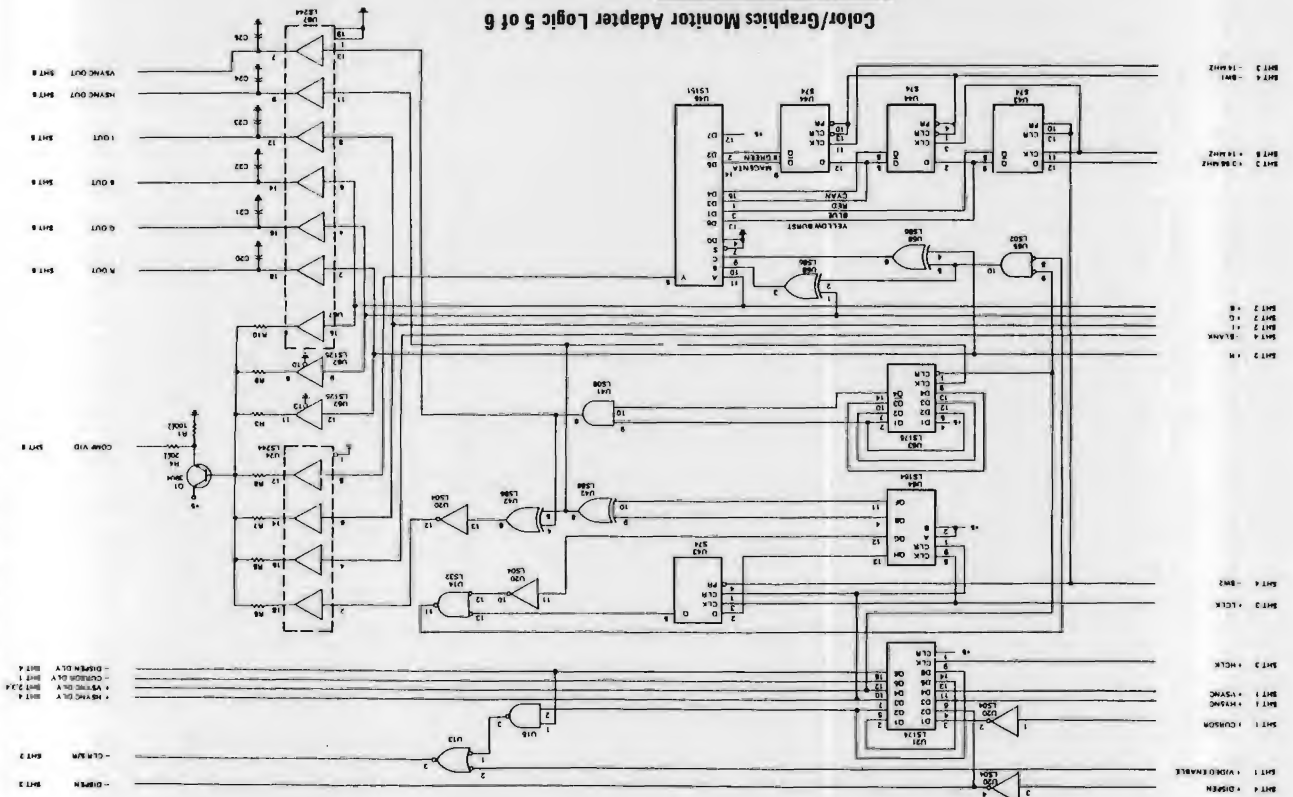
DD-28

COLOR/GRAPHICS MONITOR ADAPTER



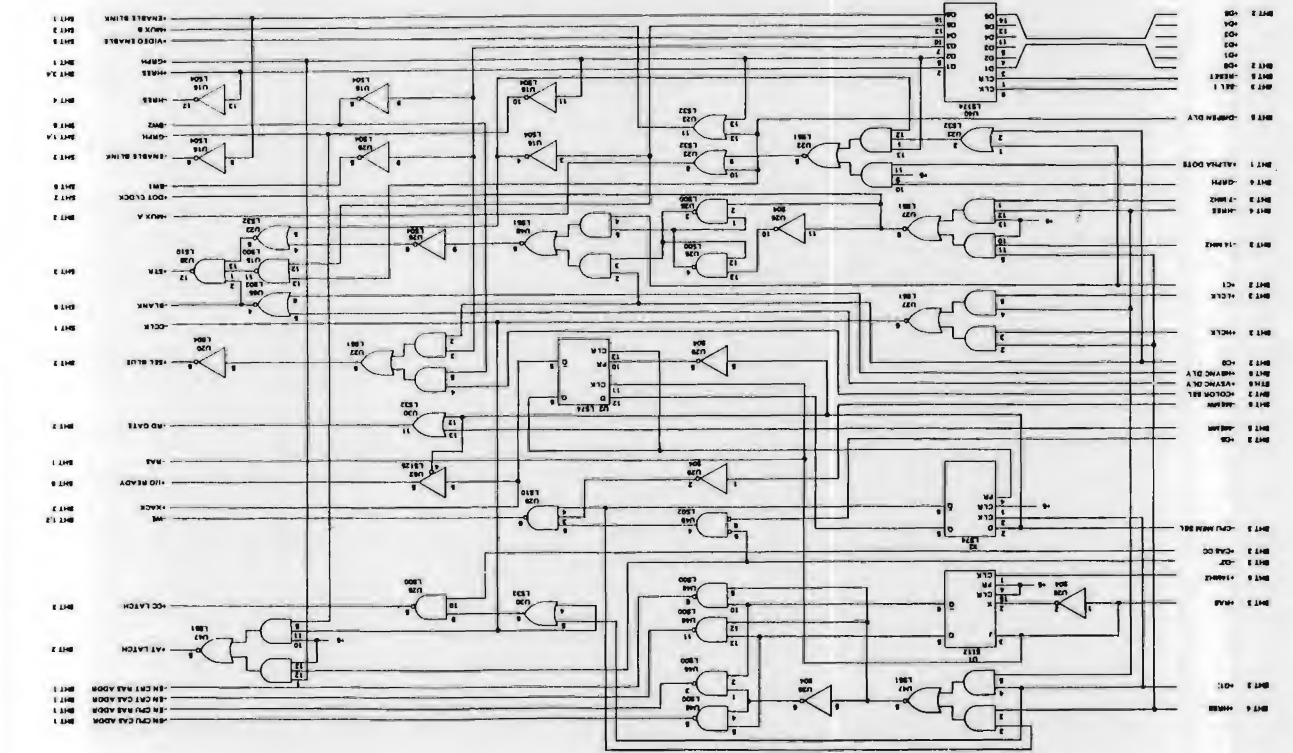
Color/Graphics Monitor Adapter Logic 5 of 6

COLOR/GRAPHICS MONITOR ADAPTER



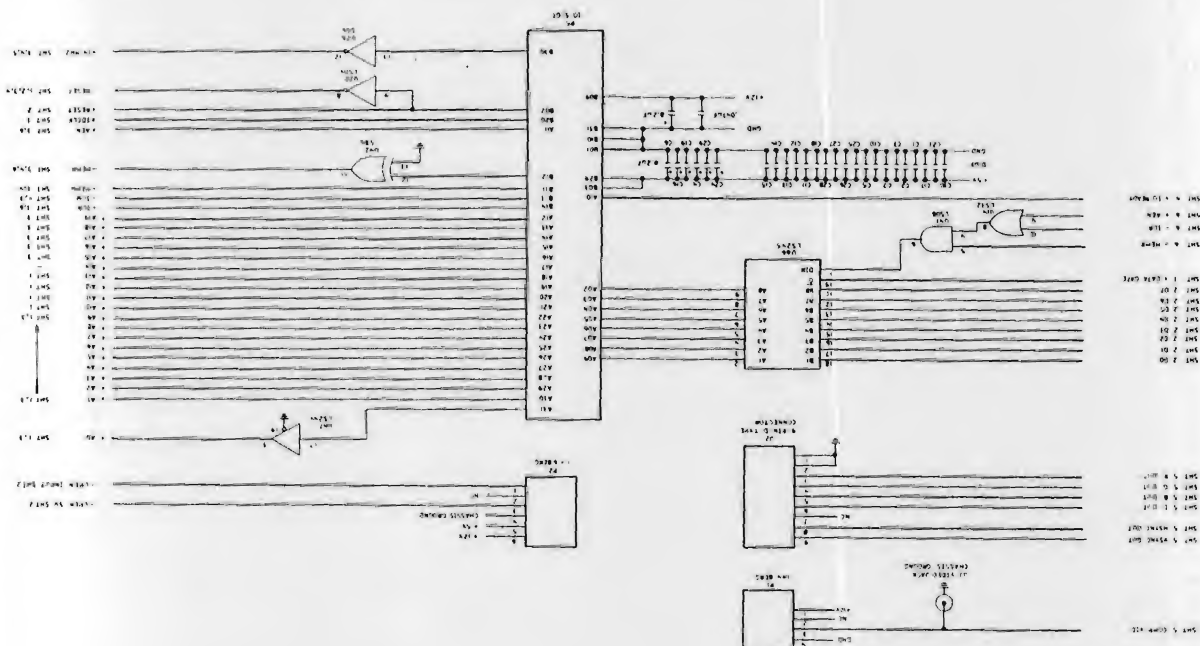
Color/Graphics Monitor Adapter Logic 4 of 6

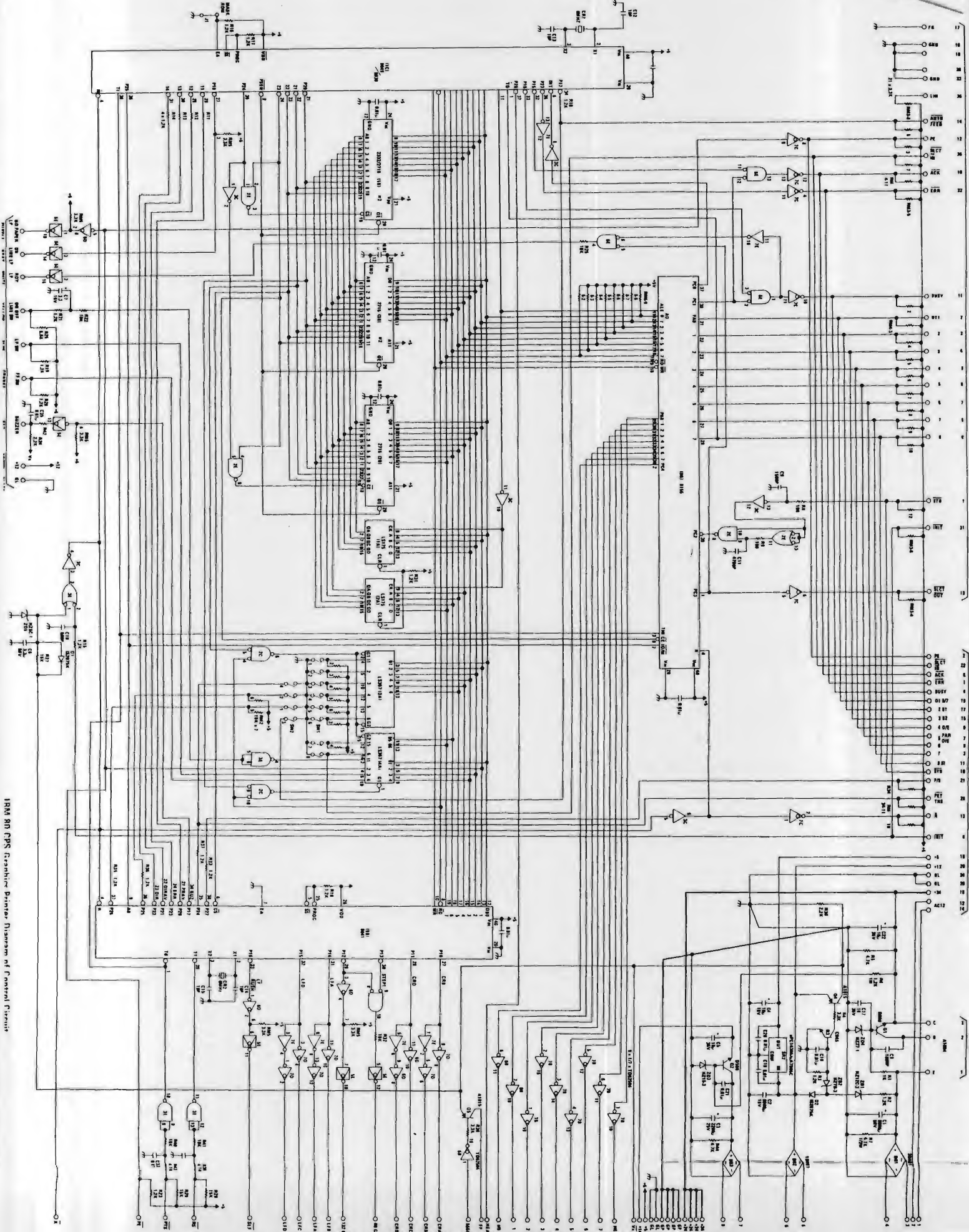
COLOR/GRAPHICS MONITOR ADAPTER



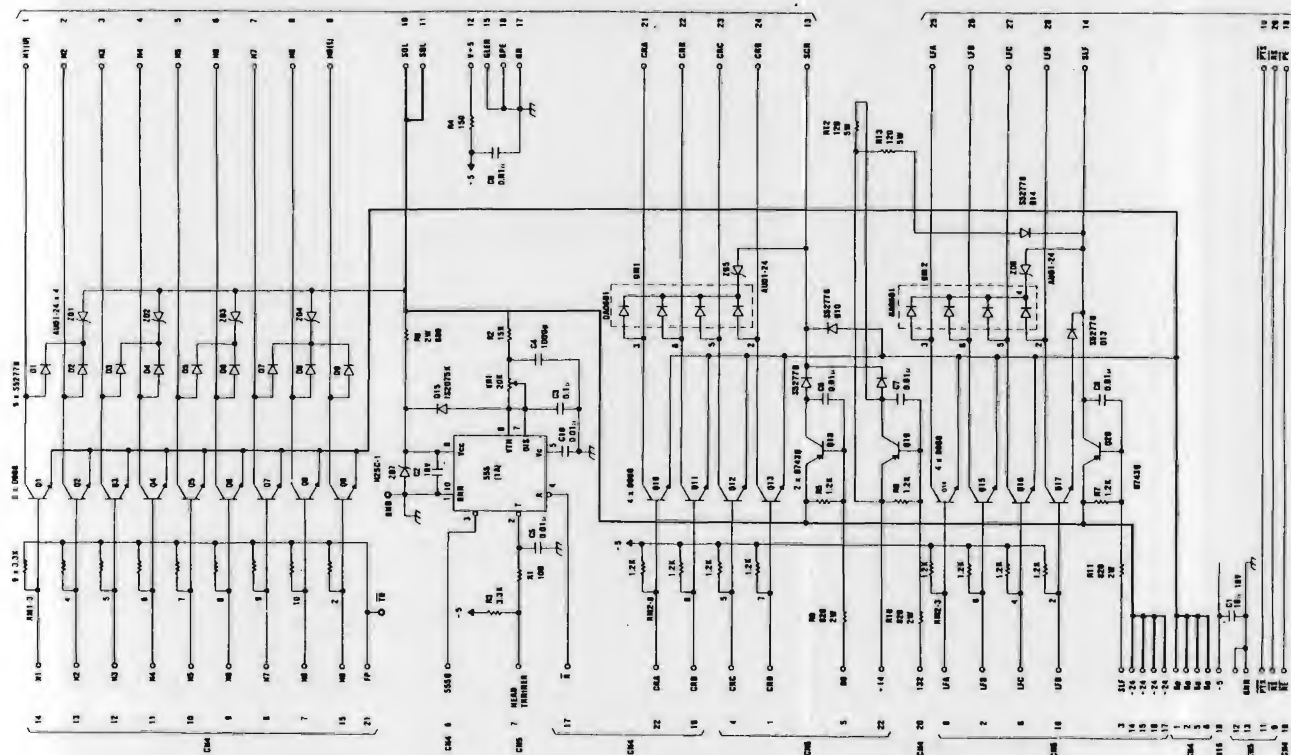
COLOR/GRAPHICS MONITOR ADAPTER

Color/Graphics Monitor Adapter Logic 6 of 6

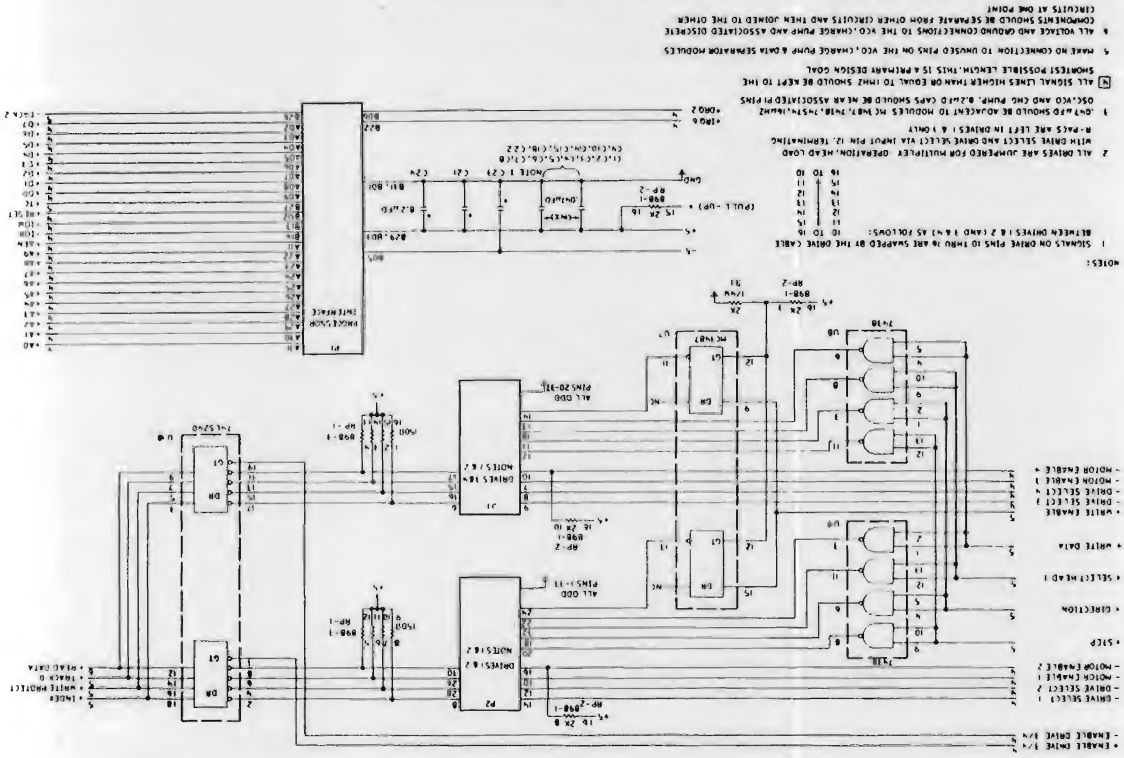




IBM 80 CPS Diagram of Driver Circuit Graphics Printer



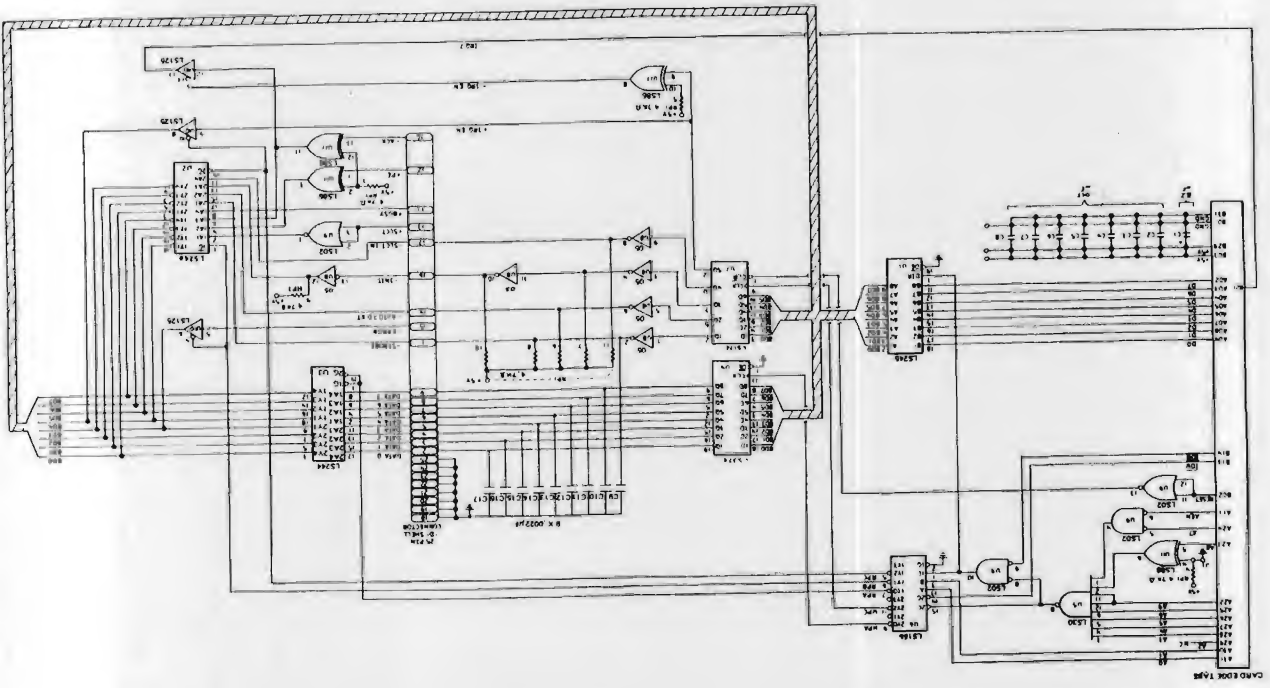
5 1/4" Diskette Drive Adapter Logic 3 of 6



Note: Logics one and two of six are not applicable.

5 1/4" DISKETTE DRIVE ADAPTER

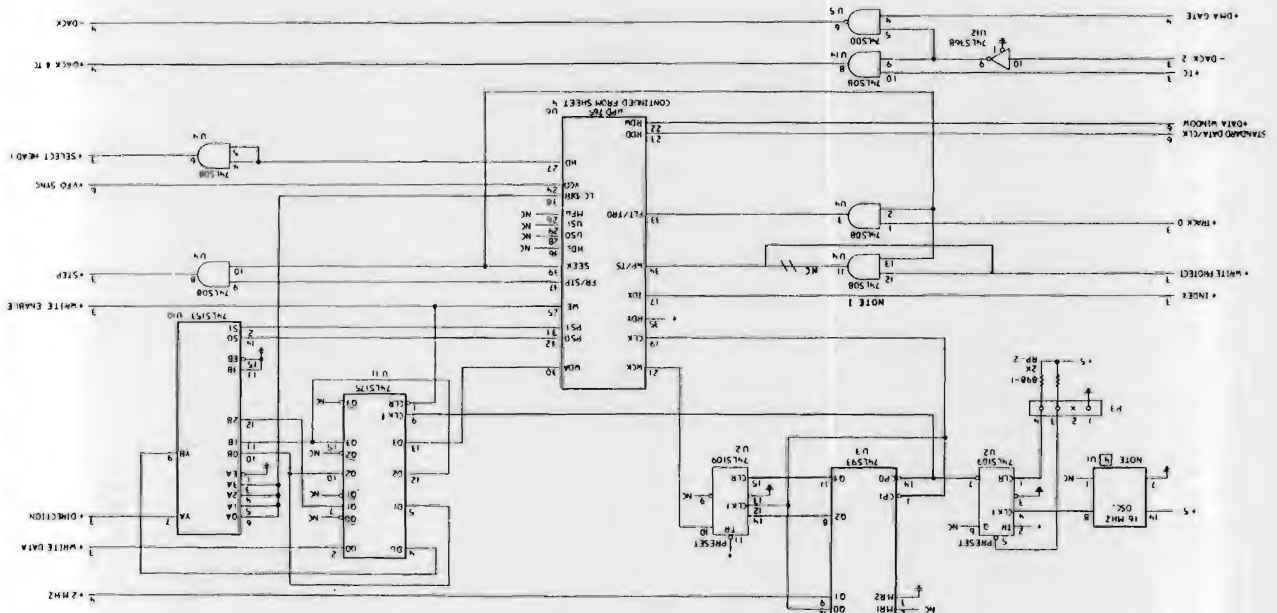
Parallel Printer Adapter



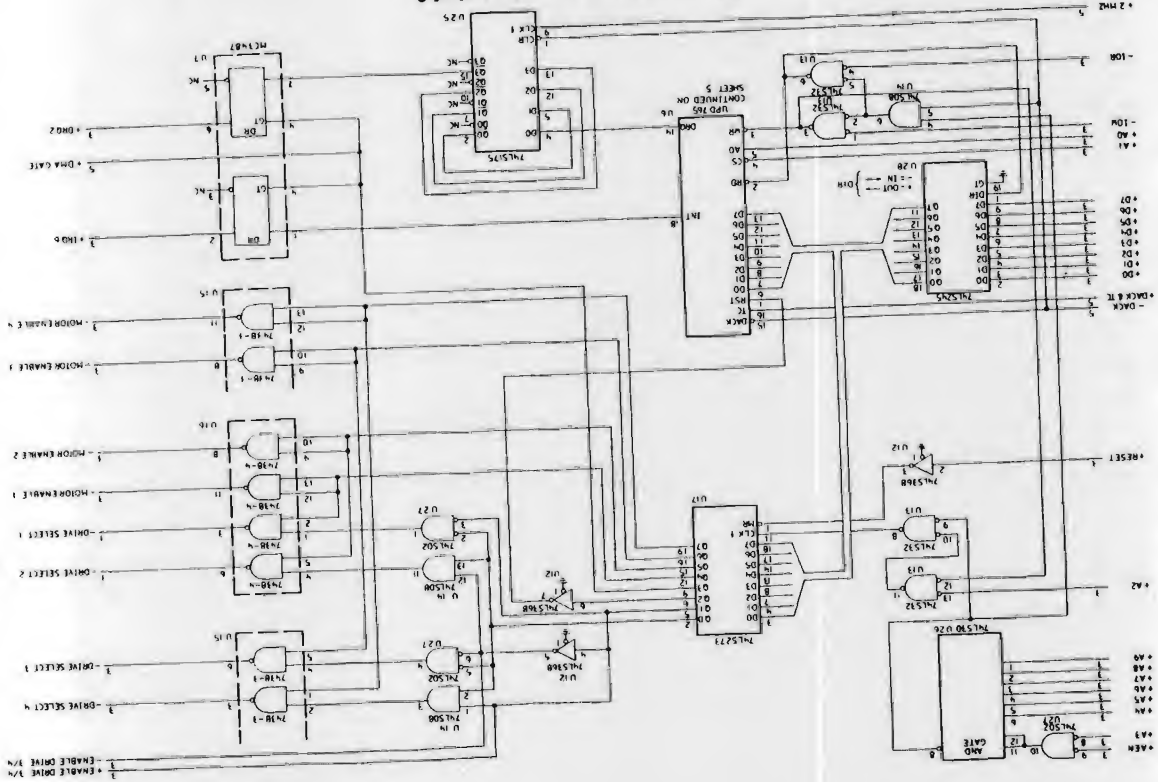
PARALLEL PRINTER ADAPTER

5 1/4" Diskette Drive Adapter Logic 5 of 6

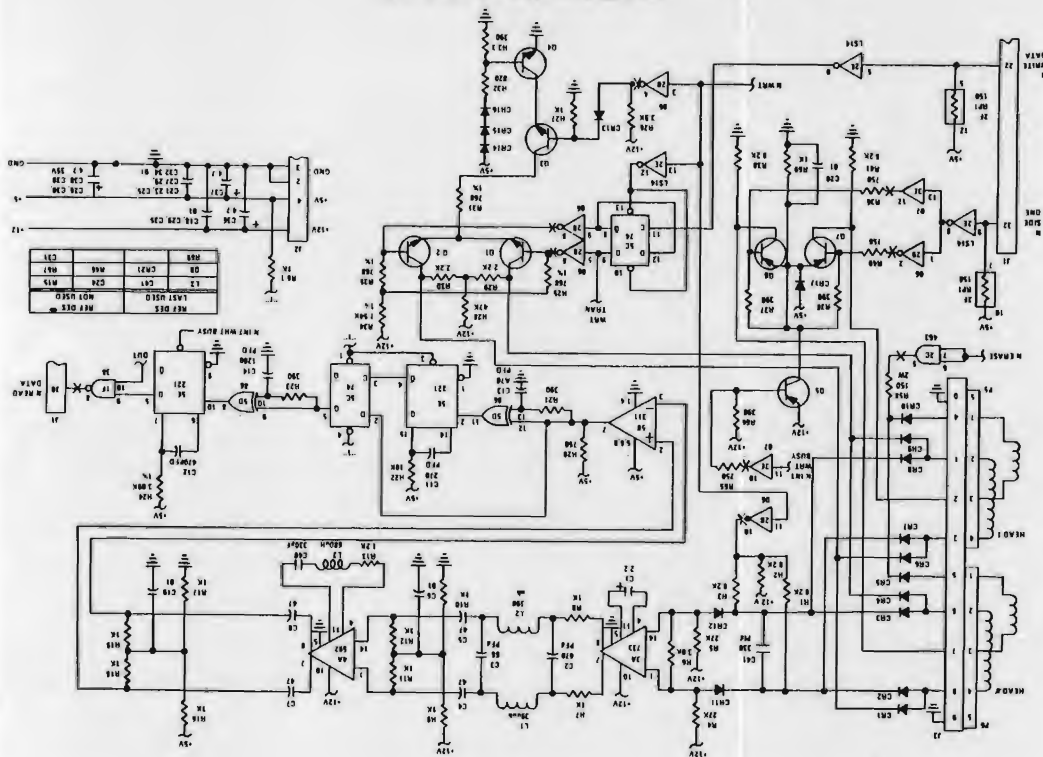
NOTE: 04 (74LS08) PINS 12 AND 13 ARE
CONNECTED ONLY ON CARDS
BUILT USING MAY CARD PM5001293



5% "Diskette Drive Adapter Logic 4 of 6

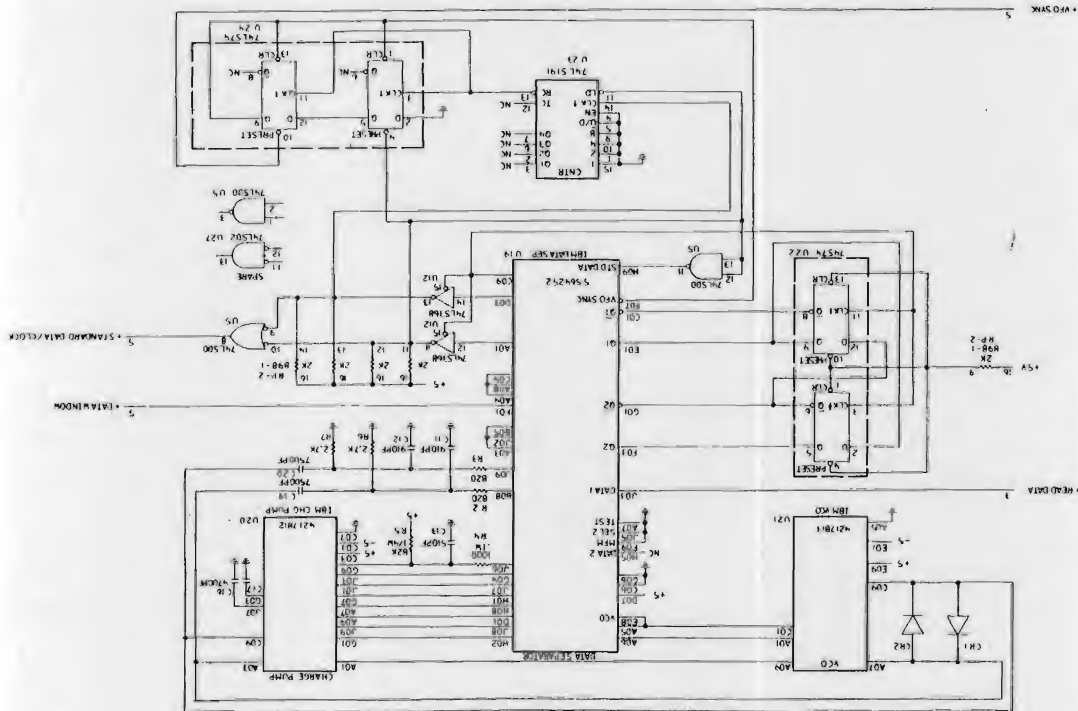


5 1/4" Diskette Drive Logic 1 of 3



5 1/4" DISKETTE DRIVE

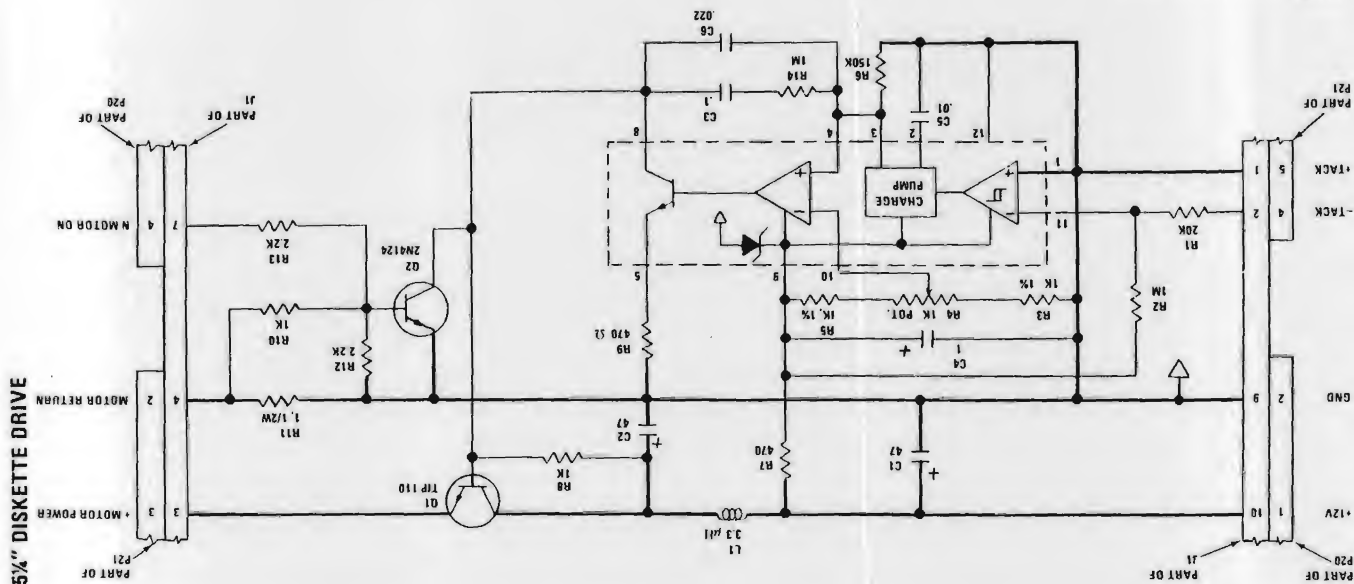
5 1/4" Diskette Drive Adapter Logic 6 of 6



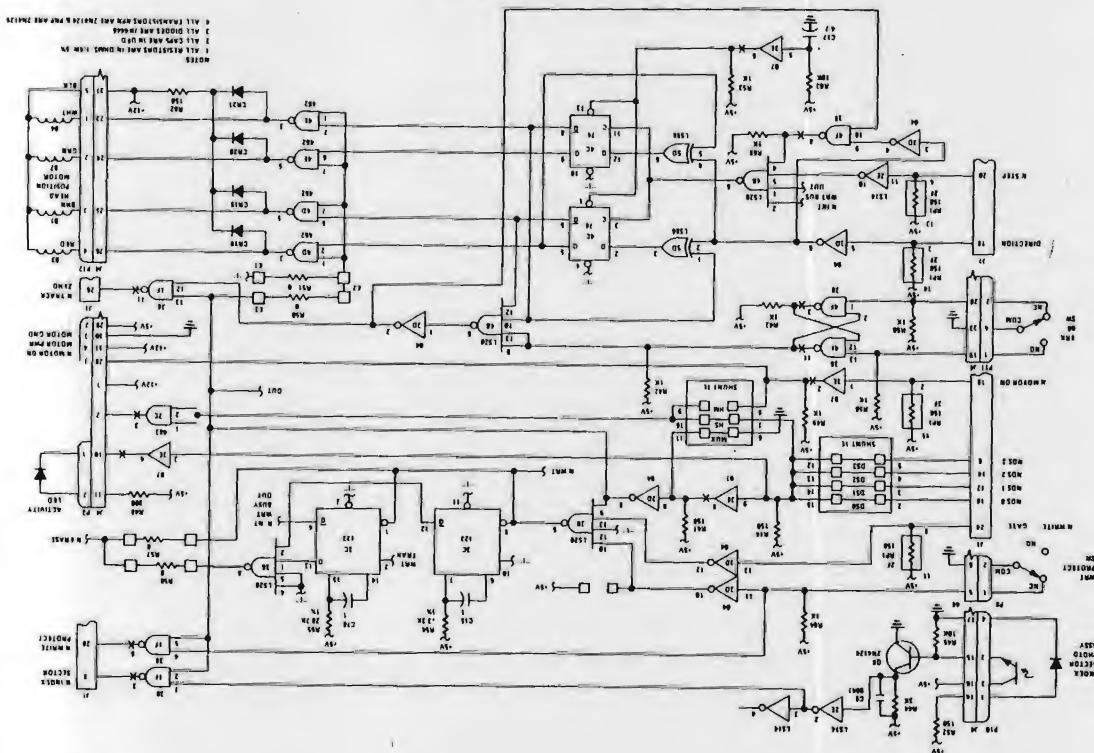
5 1/4" DISKETTE DRIVE ADAPTER

5 1/4" Diskette Drive Logic 3 of 3

NOTES:
1. RESISTORS ARE IN OHMS, 5%, 1/4 W.
2. 1% RESISTORS ARE 1/8 W.
3. CAPACITORS ARE IN μ F, 20%, 35 V.



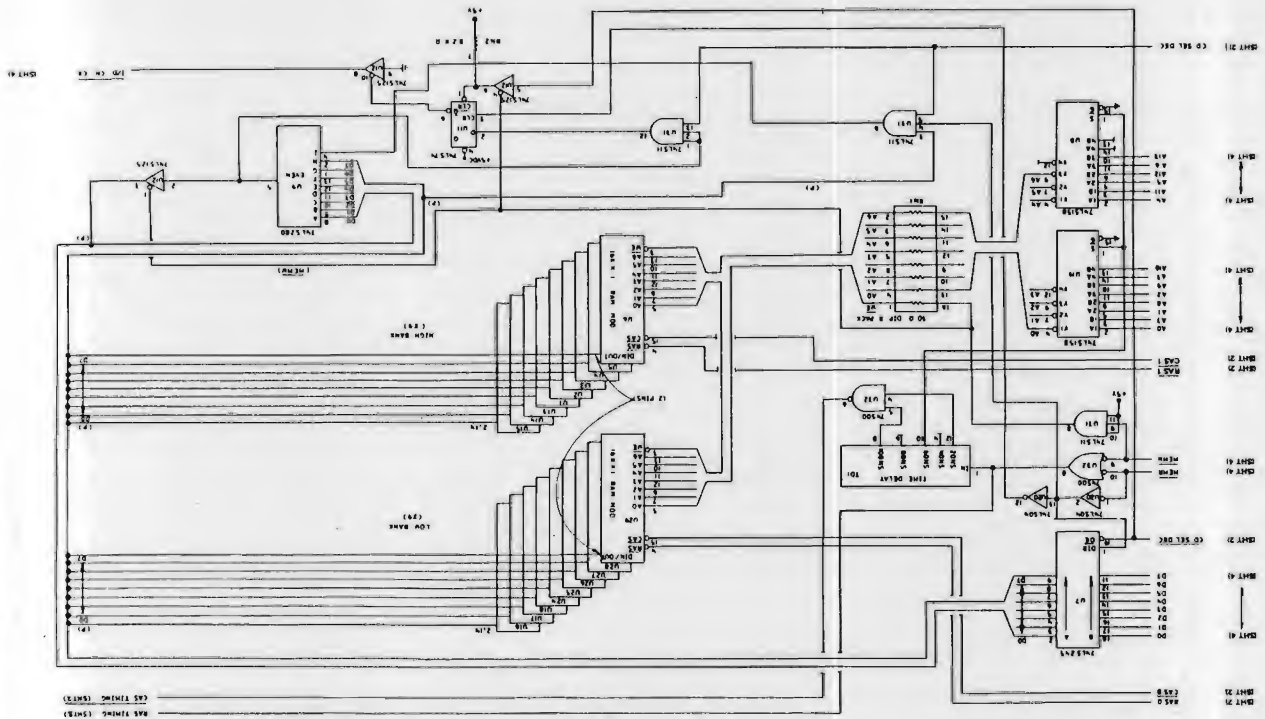
5 1/4" Diskette Drive Logic 2 of 3



5 1/4" DISKETTE DRIVE

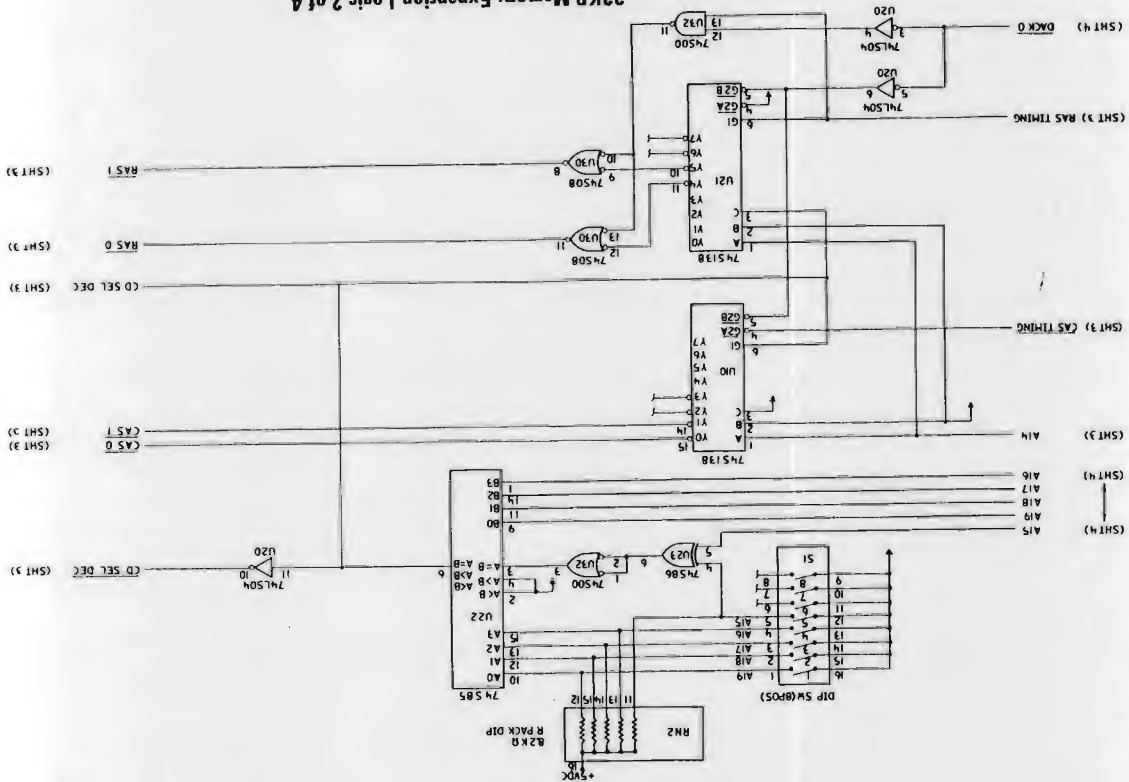
32KB Memory Expansion Logic 3 of 4

32 KB MEMORY EXPANSION



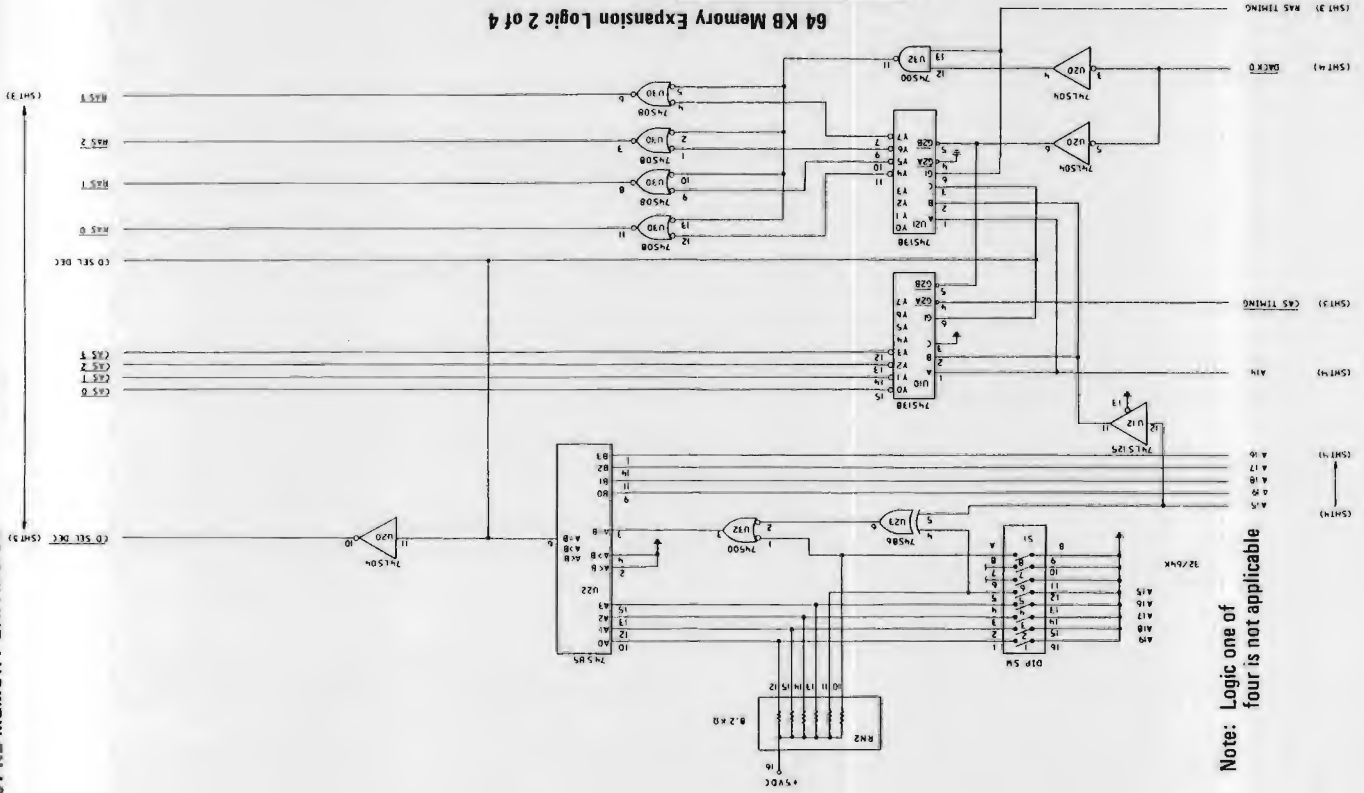
32KB Memory Expansion Logic 2 of 4

32 KB MEMORY EXPANSION

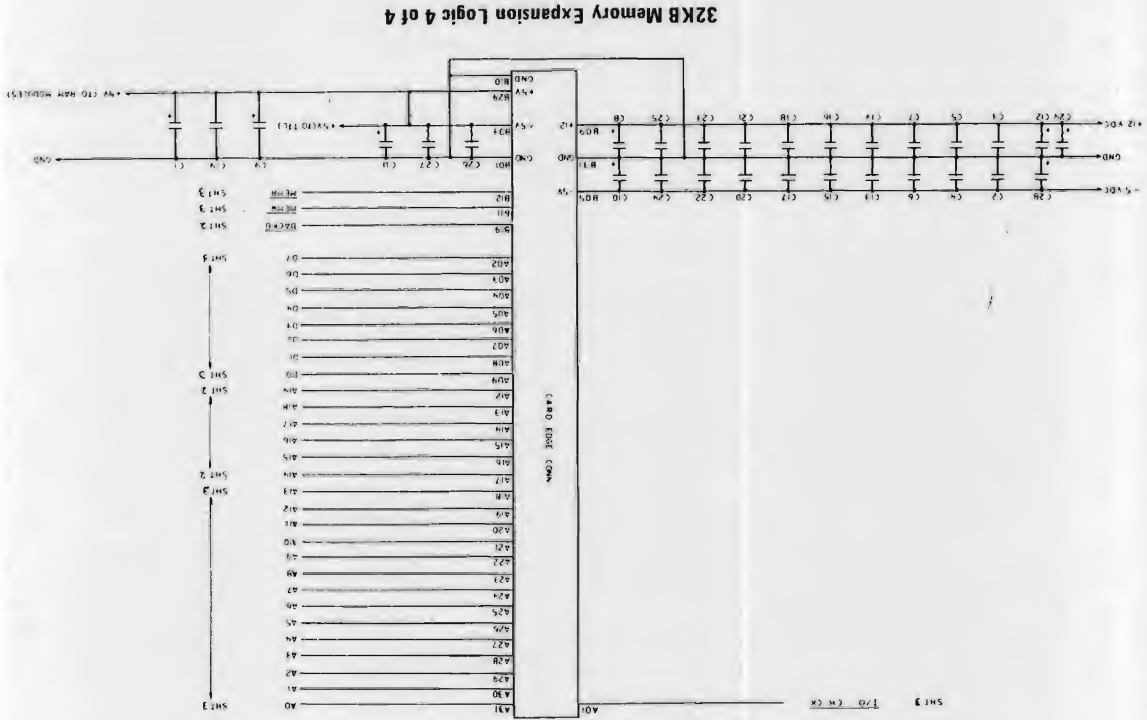


Note: Logic one of four is not applicable

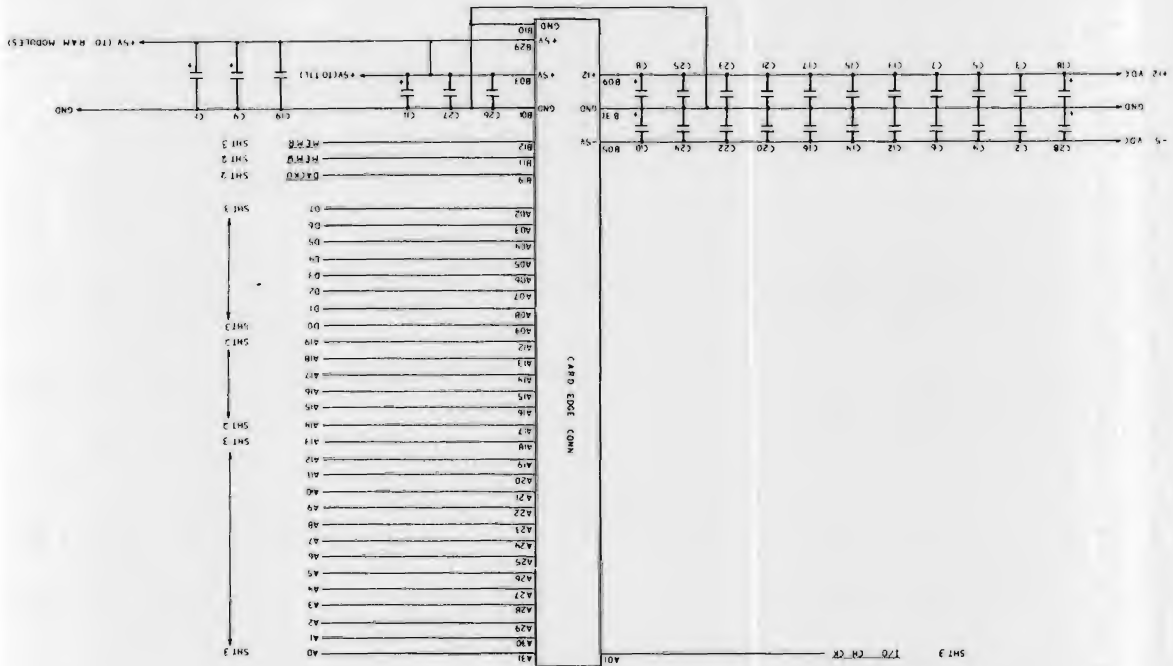
64 KB MEMORY EXPANSION



32KB MEMORY EXPANSION

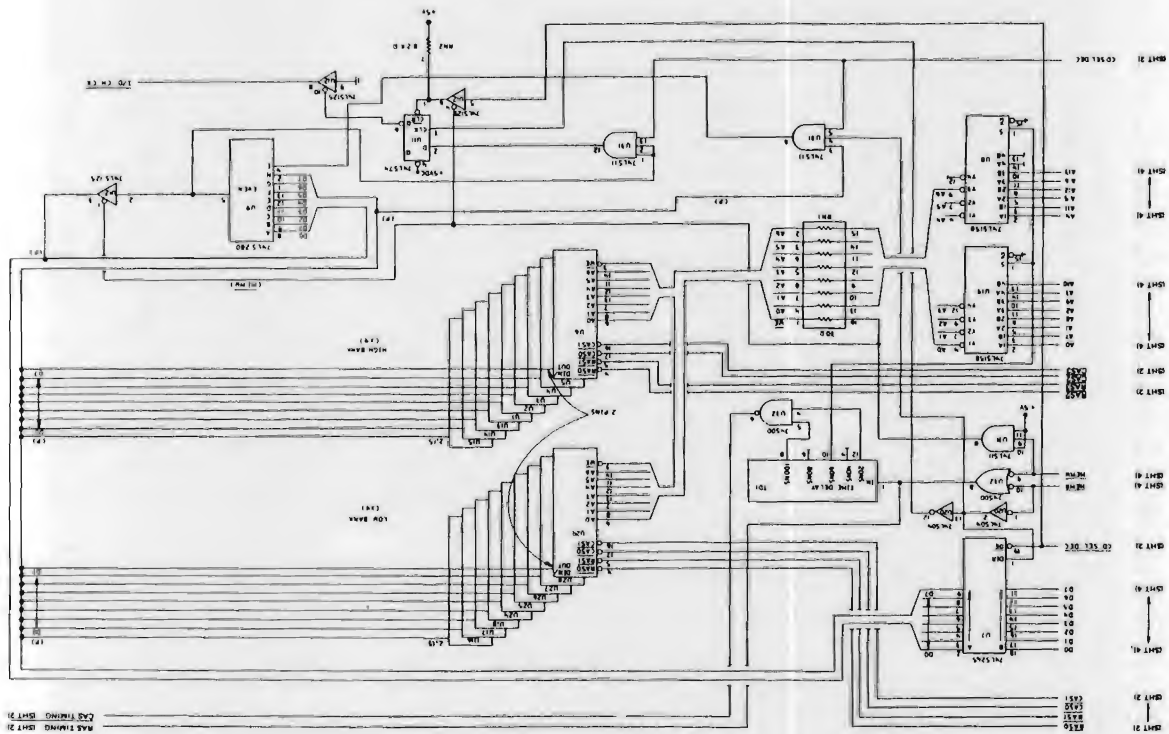


64 KB Memory Expansion Logic 4 of 4

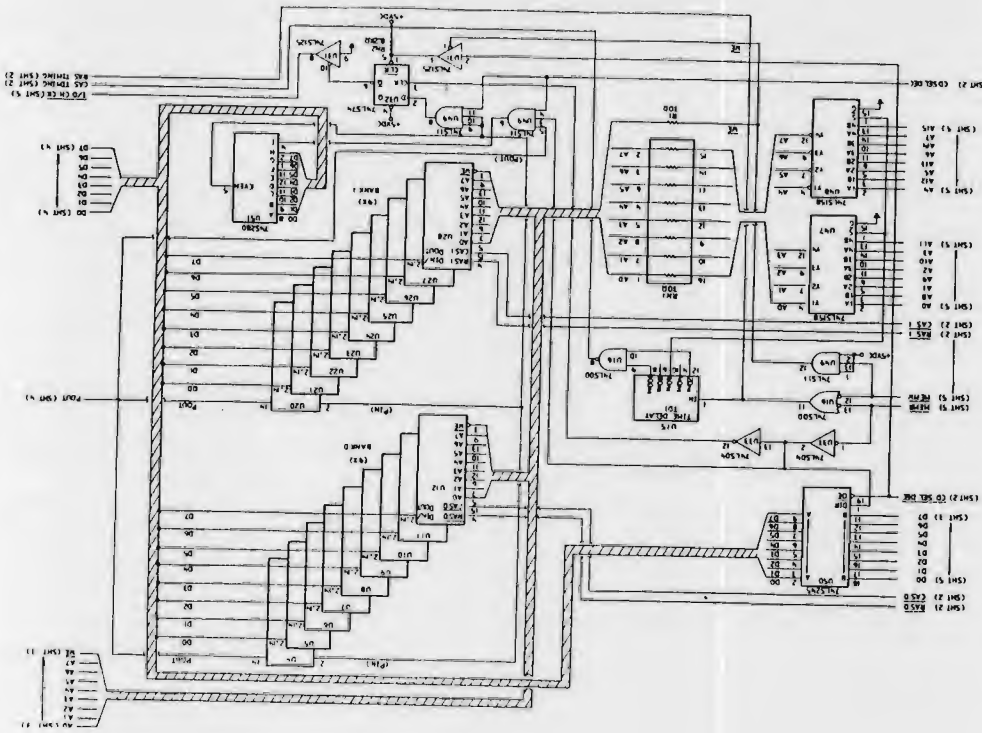


64 KB MEMORY EXPANSION

64KB Memory Expansion Logic 3 of 4

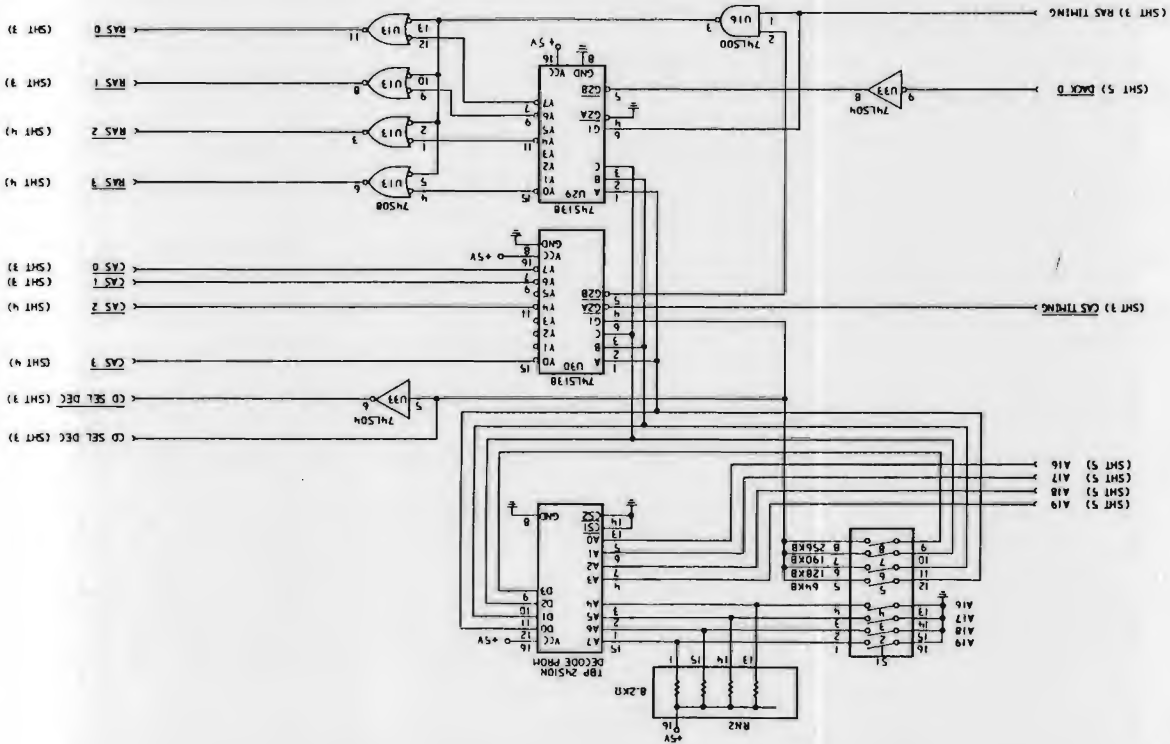


64 KB MEMORY EXPANSION

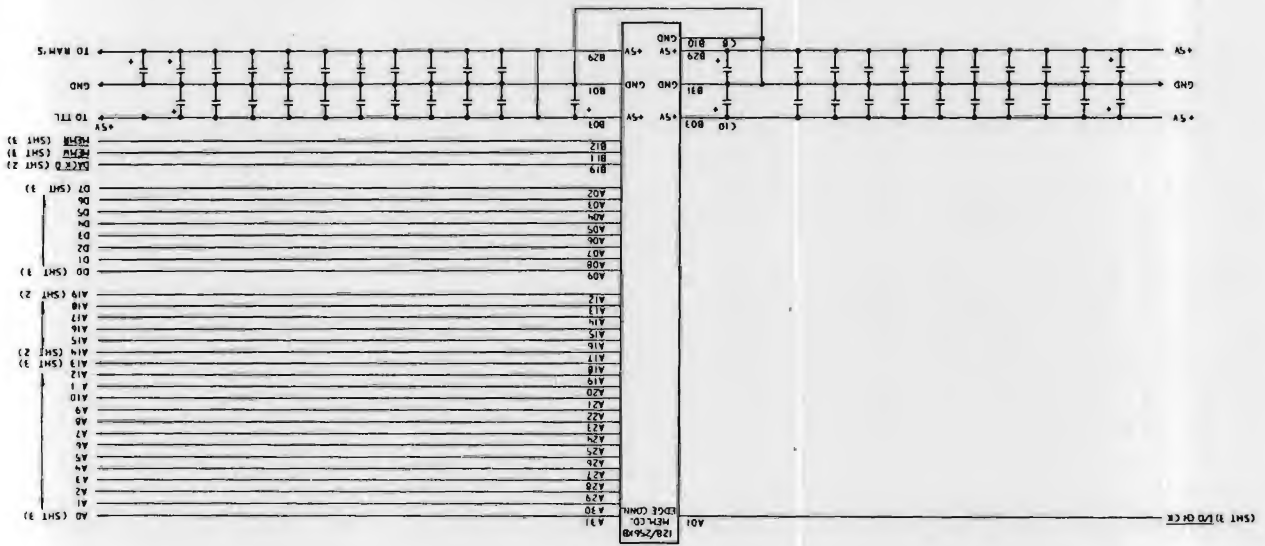


64/256KB MEMORY EXPANSION OPTION

64/256KB Memory Expansion Logic 1 of 4

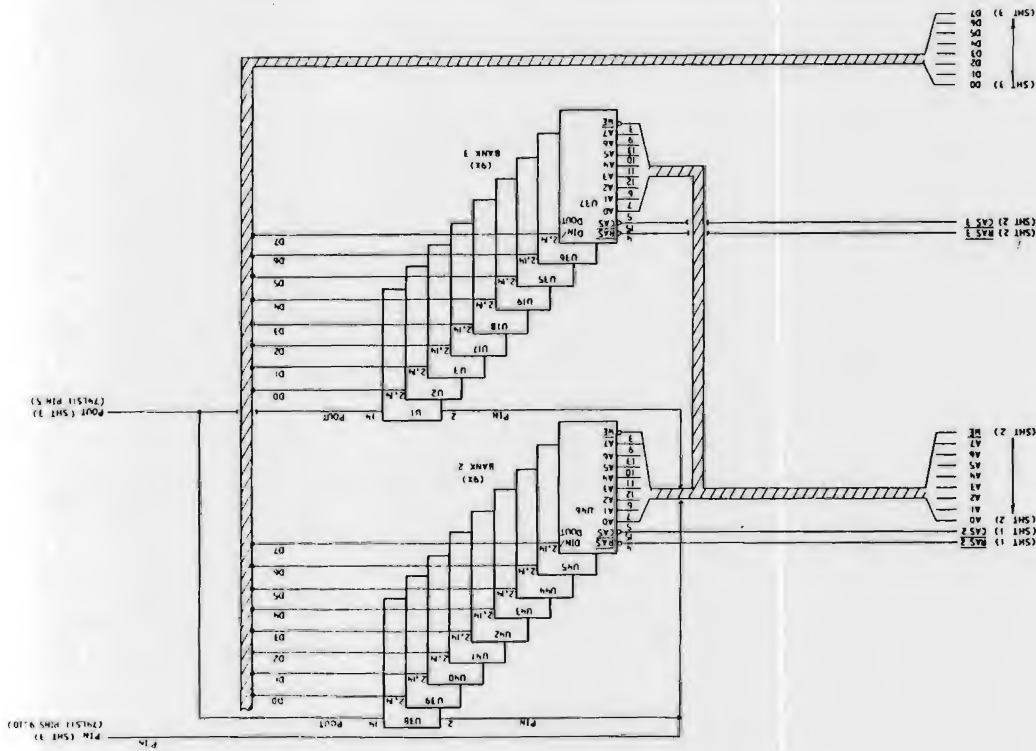


64/256KB MEMORY EXPANSION OPTION



64/256KB MEMORY EXPANSION OPTION

64/256KB Memory Expansion Logic 3 of 4

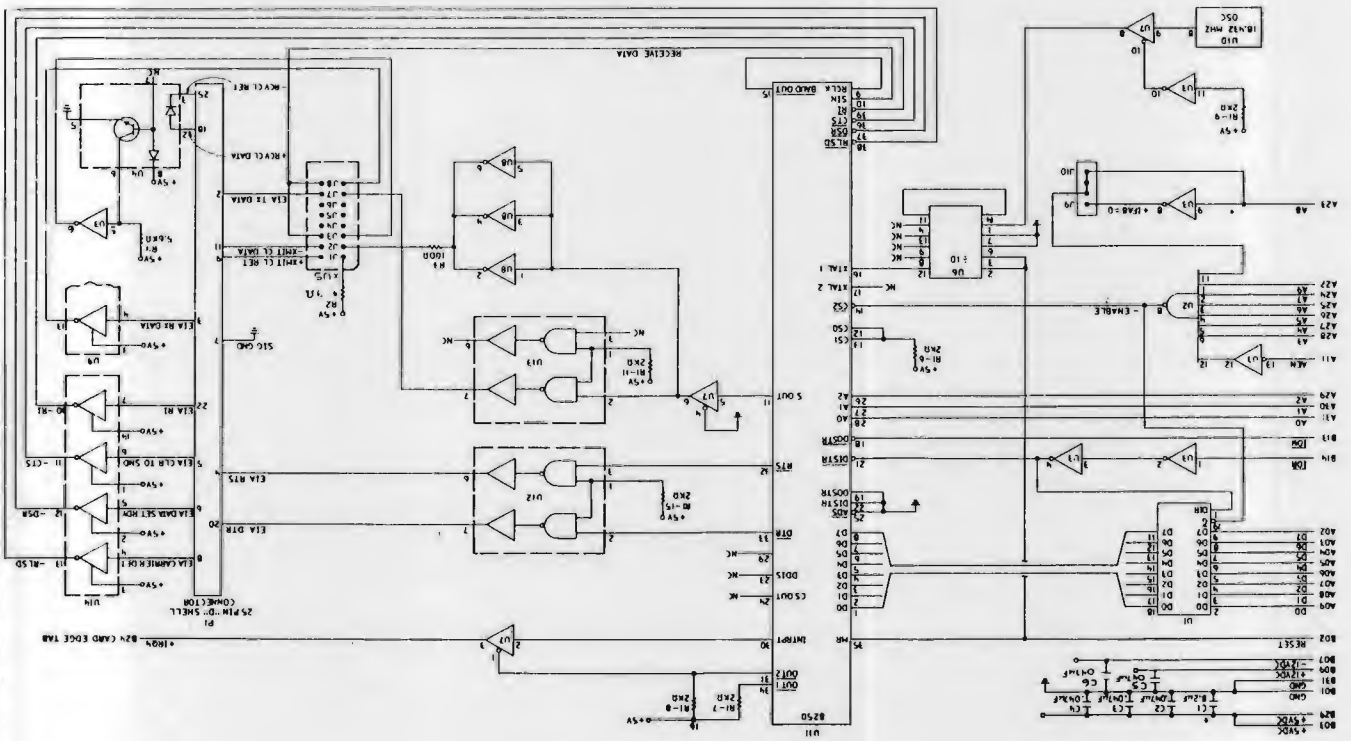


64/256KB MEMORY EXPANSION OPTION

D-54



ASYNCHRONOUS COMMUNICATIONS ADAPTER



APPENDIX E. UNIT SPECIFICATIONS

System Unit

Size:

Length—19.6" (500 mm)
Depth—16.1" (410 mm)
Height—5.5" (142 mm)

Weight:

Without Diskette Drive Unit—20.9 lbs (9.5 kg)
With Diskette Drive Unit—25 lbs (11.4 kg)

Power Cable:

Length—6'0" (1.83 m)
Size—18 AWG

Environment:

Air Temperature

System ON, 60° to 90° F (15.6° to 32.2° C)
System OFF, 50° to 110° F (10° to 43° C)

Humidity

System ON, 8% to 80%
System OFF, 20% to 80%
Heat Output, 1083 BTU/HR (Maximum)

Noise Levels:

Without Printer, 59 DBS
With Printer, 66 DBS

Electrical:

Nominal—120 VAC
Minimum—104 VAC
Maximum—127 VAC
KVA—3175 maximum
OR
220/240 VAC
180 VAC
259 VAC
KVA—3175 maximum

Keyboard

Size:

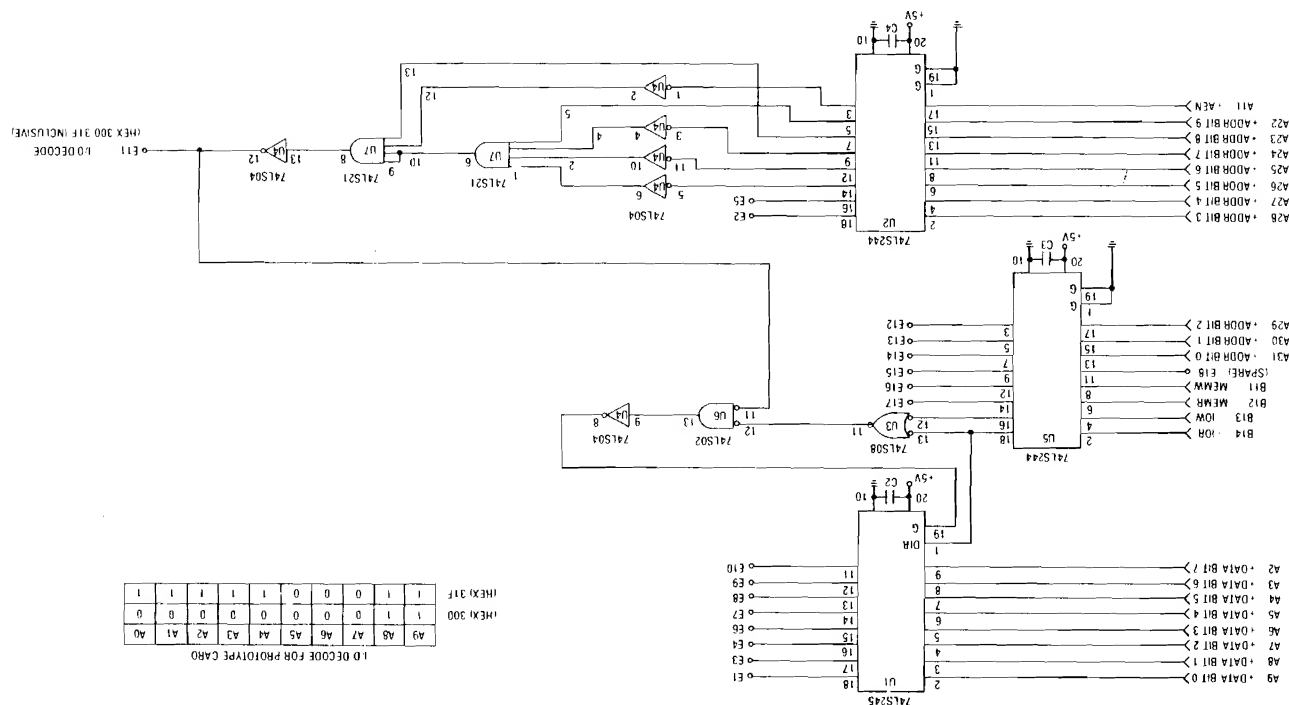
Length—19.6" (500 mm)
Depth—7.87" (200 mm)
Height—2.2" (57 mm)

Weight:

6.5 lbs (14.3 kg)

PROTOTYPE CARD INTERFACE DIAGRAM

Prototype Card Interface Diagram



IBM Monochrome Display

Size:

Length—14.9" (380 mm)
Depth—13.7" (350 mm)
Height—11" (280 mm)

Weight:

17.3 lbs (7.9 kg)

Heat Output:

325 BTU/HR

Power Cable:

Length—3'0" (914 mm)
Size—18 AWG

Signal Cable:

Length—4'0" (1.22 m)
Size—22 AWG

IBM 80 CPS Graphics Printer

Size:

Width—14.7" (374 mm)
Depth—12.0" (305 mm)
Height—4.2" (107 mm)

Weight:

12.0 lbs (5.5 kg)

Power Cable:

Length—6'0" (1.83 m)
Size—18 AWG

Signal Cable:

Length—6'0" (1.83 m)
Size—22 AWG

Heat Output:

341 BTU/HR (Max.)

Electrical (three models available)

Nominal-	120 VAC	220 VAC	240 VAC
Minimum-	104 VAC	198 VAC	216 VAC
Maximum-	127 VAC	242 VAC	264 VAC

GLOSSARY

1. **Address Buss:** A set of wires or signals carrying the binary-coded address from the Intel-8088 microprocessor throughout the rest of the IBM Personal Computer System Unit.
2. **AEN:** Address Enable. (Refer to System Board I/O Channel Descriptions).
3. **ALE:** Address Latch Enable. (Refer to System Board I/O Channel Descriptions).
4. **Analog:** (1) Pertaining to representation by means of continuously variable physical quantities. (2) Contrast with digital.
5. **A/N:** Alphanumeric: Pertaining to a character set that contains letters, digits, and usually other characters, such as punctuation marks. Synonymous with alphanumeric.
6. **A0-A19:** Address bits 0-19. (Refer to System Board I/O Channel Descriptions).
7. **APA:** All points addressable graphics.
8. **ASCII:** American Standard Code of Information Interchange. The standard code, using a coded character set consisting of 7-bit coded characters (8 bits including parity check), used for information interchange among data processing systems, data communication systems and associated equipment. The ASCII set consists of control characters and graphic characters.
9. **Assembler:** A computer program used to assemble. Synonymous with assembly program.
10. **BASIC:** (Beginner's all-purpose symbolic instruction code). A programming language with a small repertoire of commands and a simple syntax, primarily designed for numerical application.
11. **BAUD:** (1) A unit of signaling speed equal to the number of discrete conditions or signal events per second in Morse code, one bit per second in a train of binary signals, and one 3-bit value per second in a train of signals each of which can assume one of eight different states. (2) In asynchronous transmission, the unit of modulation rate corresponding to one unit of interval per second, i.e. if the duration of the unit interval is 20 milliseconds, the modulation rate is 50 baud.

12. Binary: (1) Pertaining to a selection, choice, or condition that has two possible values or states. (2) Pertaining to a fixed radix numeration system having a radix of two.
13. BIOS: Basic Input/Output System.
14. Bootstrap: A technique or device designed to bring itself into a desired state by means of its own action, e.g. a machine routine whose first few instructions are sufficient to bring the rest of itself into the computer from an input device.
15. Buffer: An area of storage that is temporarily reserved for use in performing an input/output operation, into which data is read or from which data is written. Synonymous with I/O area. A portion of storage for temporarily holding input or output data.
16. Bus: One or more conductors used for transmitting signals or power.
17. Byte: (1) A binary character operated upon as a unit and usually shorter than a computer word. (2) The representation of a character.
18. CLK: Clock. (Refer to System Board I/O Channel Descriptions).
19. Code: (1) A set of unambiguous rules specifying the manner in which data may be represented in a discrete form. Synonymous with coding scheme. (2) A set of items such as abbreviations representing the members of another set. (3) Loosely, one or more computer programs, or part of a computer program. (4) To represent data or a computer program in a symbolic form that can be accepted by a data processor.
20. Computer: A data processor that can perform substantial computation, including numerous arithmetic operations, or logic operations, without intervention by a human operator during the run.
21. CPS: Characters per second.
22. CRC: The cyclic redundancy check character.
23. CRT: (1) A Cathode ray tube display. (2) A display device, such as the IBM Monochrome Display, that uses a cathode ray tube.
24. CTS: Conversational Terminal System. (2) Clear to Send. Associated with modem control.
25. DACK0-DACK3: DMA Acknowledge 0 to 3. (Refer to System Board I/O Channel Description.)
26. Data: (1) A representation of facts, concepts or instructions in a formalized manner suitable for communication, interpretation, or processing by humans or automatic means. (2) Any representations such as characters or analog quantities to which meaning is, or might be assigned.
27. Din Connectors: One of the connectors specified by the Din standardization committee.
28. DIP: "Dual In-Line Package." A widely used container for an integrated circuit. DIP's are pins usually in two parallel rows. These pins are spaced on 1/10" inters and come in different configurations ranging from a 14-pin assembly to a 40-pin configuration.
29. Display: A visual presentation of data.
30. DMA: Direct Memory Access.
31. DO-D7: Data Bits 0 to 7. (Refer to System Board I/O Channel Descriptions.)
32. DRQ1-DRQ3: DMA Request 1 to 3. (Refer to System Board I/O Channel Descriptions.)
33. DSR: Data Set Ready, associated with modem control.
34. DTR: Distribution Tape Reel.
35. Edge Connector: An opening which joins with the end of a circuit board. The purpose of this interface is to send electrical signals back and forth.
36. EIA/CCITT Drives: Electronic Industries Association/Consultative Committee on International Telegraphy and Telephony Drives.
37. EPROM or 'PROM': Term for "Programmable Read-Only Memory." An EPROM or 'PROM' is actually Read-Only Memory (ROM) but the contents may be changed by electrical means. EPROM or 'PROM' information is not destroyed when the power is cut off.
38. Firmware: Memory chips with the software programs already built in.
39. Graphics: Symbols Produced by a process such as handwriting, drawing or printing. Synonymous with graphic symbol.
40. Hexadecimal: Pertaining to a selection, choice, or condition that has sixteen possible values or states. These values or states usually contain 10 digits and six letters A through F. Hexadecimal digits are equivalent to a power of 16.

41. Hertz (Hz): A unit of frequency equal to one cycle per second.
42. High order position: The leftmost position in a string of characters.
43. Input/Output (I/O): Pertaining to a device or to a channel that may be involved in an input process, and, at a different time, in an output process. (2) Pertaining to a device whose parts can be performing an input process and an output process at the same time.
44. Integrated Circuit: A combination of interconnected circuit elements inseparably associated on or within a continuous substrate.
45. Interpreter: A computer program used to interpret. Synonymous with interpretive program.
46. Interrupt: (1) A suspension of a process, such as the execution of a computer program, in such a way that the process can be resumed. (2) To stop a process in such a way that it can be resumed. (3) In data transmission, to take an action at a receiving station that causes the transmitting station to terminate a transmission.
47. I/O Channel: Input/Output Channel. In a data processing system, a functional unit, controlled by the processing unit, that handles the transfer of data between main storage and peripheral equipment.
48. I/O CH CK: I/O-Channel Check. (Refer to System Board I/O Channel Descriptions.)
49. I/O CH RDY: I/O Channel Ready. (Refer to System Board I/O Channel Descriptions.)
50. IMR: Interruption Mask Register.
51. IOR: I/O Read Command. (Refer to System Board I/O Channel Descriptions.)
52. IOW: I/O Write Command. (Refer to System Board I/O Channel Descriptions.)
53. IRQ2-IRQ7: Interrupt Request 2 to 7. (Refer to System Board I/O Channel Descriptions.)
54. K: An abbreviation for the prefix kilo, i.e. 1000 in decimal notation. To the tenth power, 1024 in decimal notation.
55. KB: Kilobyte.
56. Khz: Kilohertz. A unit of frequency equal to 1,000 hertz.

57. Low order position: The rightmost position in a string of characters.
58. Machine Language: (1) A language that is used directly by a machine. (2) Another term for computer instruction code.
59. Memory Address: A two-byte value selecting one specific memory location on a memory map.
60. Memory Location: The most specific part of a memory map that the computer can refer to.
61. Memory Map: The list of memory locations addressed directly by the microprocessor.
62. MEMR: Memory Read Command. (Refer to System Board I/O Channel Descriptions.)
63. MEMW: Memory Write Command. (Refer to System Board I/O Channel Descriptions.)
64. MFM Coded: Modified Frequency Modulation. It is double density encoding of information on a diskette.
65. Mhz: Megahertz. A unit of frequency equal to one million Hertz.
66. Microprocessor: A processing unit, or part of a processing unit, that consists of microcode. In the IBM Personal Computer, the microprocessor is the Intel-8088.
67. Mnemonic: Symbol or symbols used instead of terminology more difficult to remember. Usually a mnemonic has two or three letters.
68. Mode: (1) A method of operation, for example, the binary mode, the interpretive mode, the alphanumeric mode. (2) The most frequent value in the statistical sense.
69. Monitor: (1) A device that observes and verifies the operation of a data processing system and indicates any specific departure from the norm. (2) A television type display such as the IBM Monochrome Display. (3) Software or hardware that observes, supervises, controls, or verifies the operations of a system.
70. Multiplexer: A device capable of interleaving the events of two or more activities or capable of distributing the events of an interleaved sequence to their respective activities.

71. OR: A logic operator having the property that if P is a statement, Q is a statement, R is a statement..., then the OR of P,Q,R, is true if at least one statement is true, false if all statements are false. P OR Q is often represented by P+Q, PVQ. The term is synonymous with boolean add; logic add.
72. "ORed": Past tense of OR.
73. OSC: Oscillator. (Refer to System Board I/O Channel Descriptions.)
74. Output: Pertaining to a device, process, or channel involved in an output process, or to the data or states involved in an output process.
75. Personal Computer: A small home or business computer complete with a System Unit, keyboard, and available with a variety of options such as monochrome display and a dot matrix printer.
76. Pinout: A diagram of functioning pins on a pinboard.
77. Printed Circuit Board: A piece of material, usually fiberglass, which contains a layer of conductive material, usually metal. The metallic layer is then etched and electronic equipment is then attached to the fiberglass. The electronic equipment then has the capacity to transmit electronic signals through the board by way of the etched metal tracks.
78. Program: (1) A series of actions designed to achieve a certain result. (2) To design, write and test computer programs.
79. Read/Write Memory: Random access storage.
80. Reset Drv: Reset Driver. (Refer to System Board I/O Channel Descriptions.)
81. RF Modulator: The device used to convert the composite video signal to the antenna level input of a home TV.
82. ROM: Read-only Memory.
83. ROM BIOS: Read-only Memory/Basic Input Output System.
84. RS 232 Port: Asynchronous Type Communications.
85. RTS: Ready to Send. Associated with modem control.

86. Scan Line: The use of a cathode beam to test the cathode ray tube of a display used with a personal computer.
87. Schematic: The description, usually in diagram form, of the logical structure and physical structure of an entire data base according to a conceptual model.
88. Software: (1) Computer programs, procedures, rules, and possibly associated documentation concerned with the operation of a data processing system. (2) Contrast with hardware.
89. Strobe: (1) An instrument used to determine the exact speed of circular or cyclic movement. (2) A flashing signal displaying an exact event.
90. Text: In ASCII and data communication, a sequence of characters treated as an entity if preceded and terminated by one STX and one ETX transmission control respectively.
91. TX Data: Transmit Data. External connections of the RS 232 Asynchronous Communications Adapter interface.
92. Video: Computer data shown or displayed on a cathode ray tube monitor or display.

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